ULTRA-LOW POWER RF TRANSCEIVERS

1. Introduction

In recent years, a trend toward a world in which people will be surrounded by networked devices that are sensitive and adaptive to their needs can be foreseen. This trend has been expressed in a vision called Ambient Intelligence (AmI). It is possible to partition this world into three different classes of devices called “Watt nodes”, “milli-Watt nodes” and “micro-Watt nodes” [1].

The “Watt nodes” and the “milli-Watt nodes” demand a further improvement in technology scaling to meet the low-power target. In contrast, the design of a “micro-Watt” node requires meeting the limit of miniaturization, cost reduction and power consumption. Therefore, the complexity of this task is not in the number of transistors but in the capability to optimally combine technologies, circuit and protocol innovation to obtain the utmost simplicity of the wireless node.

At the system level there are several challenges engineers have to face to achieve such a reduction in terms of power consumption. Like in a paging channel, a low-power wake-up circuitry will be required together with RSSI measurement circuits, so that energy expenditure can be optimally adjusted. Finally, advances in energy sources and scavenging techniques are mandatory to avoid battery replacement.

2. Energy Scavenging Techniques

Several scavenging techniques have been studied in the recent years. However it is unlikely that a single solution will satisfy the total application space. For example a solar cell requires minimum lighting conditions, a piezoelectric generator sufficient vibration, and a Carnot-based

generator sufficient temperature gradient.

One of the most common scavenging techniques is to harvest energy from an RF signal. An electric field of 1 V/m yields only 0.26μW/cm^2, but such field strengths are quite rare [2]. This technique is generally used for RFID tags, which have power consumption between 1 and 100 μW. Energy can be harvested by using solar cells. While 1 cm^2 of standard solar cells produces around 100 mW under bright sun, it only generates no more than 100 μW in a typically illuminated office [2]. Also thermoelectric conversion can be used as an energy scavenging technique. Unfortunately the Carnot cycle limits the use of this technique for small temperature gradients by squeezing the efficiency below 5% for about 15 degrees temperature difference[1] [2]. Another possible solution to the scavenging problem can be found using vibrational energy. If 1 cm^3 volume is considered, then up to 4 μW power can be generated from a typical human motion, whereas 800 μW can be harvested from machine-induced stimuli [2].

Considering the aforementioned state-of-the-art in energy scavenging techniques, researchers have plenty of room for improvement both in increasing energy harvesting efficiency and in reducing the overall power consumption of wireless nodes.

3. Low-power Wireless Systems Trends

Increasing demands in wireless systems for sensing and monitoring applications have culminated in a high demand for low power autonomous devices. While AmI and the autonomous node

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[1] The Carnot efficiency is $\frac{(T_H - T_L)}{T_H}$ where TL and TH are the low and the high temperatures in Kelvin degrees. Going from the body temperature (36 degrees Celsius) to a cool room (20 degrees Celsius) the efficiency is only 5%.

concepts still are far from an everyday reality, a lot of effort has been put in the elaboration of novel standards, which can better match the low power trend. Following this novel trend, standards like Bluetooth and Zigbee have been proposed in the recent years.

Whereas these standards have reduced power consumption at expenses of a lower data-rate and Quality-of-Services (QoS), their protocol and their physical layer are still too complex to be implemented in an autonomous wireless device. Indeed, even though recently a simplified Bluetooth Low End Extension (LEE) [3] has been released, the overall transceiver power consumption remains too high for an autonomous node. While the data-rate has been scaled down to less than 0.5 Mbps and other constraints have been simplified both at the physical and MAC layer, a state-of-the-art current consumption of 9 mA (at -2 dBm transmitted power) in Tx mode and 8 mA in Rx mode have been reported for a Bluetooth transceiver [3].

In an effort to reduce the transceiver power consumption, the Zigbee standard has been recently released (preliminary standard by Philips in 2001, now updated to 802.15.4-2006). Whereas the data-rate is reduced with respect to the Bluetooth standard, the overall transceiver power consumption remains high due to complex MAC and physical layers. A recent work [4] showed a Zigbee compatible radio transceiver, with 21 mW power consumption in Rx mode and 30 mW in Tx mode (at 0 dBm output power). It follows that these standards cannot be used in the design of a "micro-Watt node" where an average power consumption of less than 100 μW and therefore, a peak power consumption lower than 10 mW, is required for duty-cycles lower than 1%

4. Recent Advances in Ultra-Low Power Transceivers

Starting with university research, the interest in ultra-low power wireless devices has increasingly spread among companies as well. In the wide scenario of ultra low-power devices, various pioneering investigations have been conducted to prove the feasibility of a "micro-Watt

node" in terms of power consumption and robustness of the communication link.

4.1.Research in industries

Several wireless products, which claim to be ultra-low power, are present on the market. Rarely these products can be used as core block for a "micro-Watt node". Pioneering researches toward the development of this kind of wireless nodes can be found in [5,6].

The Eco node [5] has been designed to monitor the spontaneous motion of preterm infants using the 2.4 GHz ISM band at 1 Mbps data-rate. While showing a good form factor (648 mm^3 by 1.6 grams), its power consumption is still far away from the minimum target required by an autonomous node. Indeed, even at 10 kbps and -5 dBm output power, it consumes 20.4 mW in Tx mode and 57 mW in Rx mode (at 1 Mbps) considering only the radio device. Whereas these nodes are designed for duty-cycled operation, as stated in Section 3, peak power consumption should not exceed 10 mW. Robustness of the link by frequency diversity is achieved by using a Frequency-Hopping Spread Spectrum (FHSS) technique.

The Telos node [6] complies with the ZigBee standard. As a result, while having a reduced data-rate (250 kbps), it has an overall power consumption of around 73 mW from 1.8 V power supply at 0 dBm transmitted power.

4.2.Research in universities

Different universities are involved in pioneering research on ultra-low power devices and networks. At Berkeley university an ultra-low power micro electro mechanical system (MEMS)-based transceiver has been developed [7]. Whereas using a 1.9 GHz carrier frequency and only two channels, the receiver power consumption is 3 mA from a 1.2 V power supply. The data rate is 40 kbps at 1.6 dBm output power. The low receiver power consumption is mainly obtained by using a high quality-factor (Q) MEMS resonator implemented as a Thin-Film Bulk Acoustic

Resonator (FBAR). If more channels are needed, like in the case of an FHSS transceiver, the hardware requirement will increase linearly with the number of channels, making this choice impractical from a low-power point of view. The transmitter part adopts direct modulation of the oscillator and MEMS technology, eliminating power hungry blocks like PLL and mixers, therefore reducing the overall power consumption. Two major drawbacks can be foreseen in the proposed architecture. While reducing the circuit and technological gap toward a "micro-Watt node", it relies on non-standard components (MEMS), which will increase the cost and will require higher driving voltage. Furthermore it lacks on robustness due to the use of only two channels, while requiring a linear increase of the power consumption with the channels number, if a more robust frequency diversity scheme has to be implemented.

At the CSEM institute the WiseNet [8] project aims to optimize both the MAC and the physical layer to obtain a robust, low-power solution for sensor networks. Whereas not using the worldwide available 2.4 GHz ISM band but the lower 433 MHz ISM band, it achieves a power consumption of only 1.8 mW from a minimum supply voltage of 0.9 V in Rx mode. This result was achieved by a combination of circuit and system innovative techniques and the use of the low-frequency 433 MHz band, which reduces the power consumption of the most power hungry blocks like the frequency synthesizer. In Tx mode a high power consumption of 31.5 mW was reported mainly due to the choice of a high output power of 10 dBm. Data-rate is 25 kbps with frequency-shift keying (FSK) modulation.

The proposed solution, while relying partially on the frequency band choice to reduce the power consumption, still requires external components like high-Q inductors for the LC-tank circuit and external RF filters, which will deteriorate form-factor and power consumption at higher frequencies.

5. System Level Aspects for Wireless Micro-sensor Nodes

Receiver sensitivity depends on the noise figure (NF), noise bandwidth and the required signal-to-noise ratio (SNR) of the demodulator. The NF depends on the receiver architecture and technology used and in an asymmetric scenario can be considered to be smaller than 10 dB. The required SNR depends on the modulation scheme and so no improvement can be expected given a certain bit error rate (BER) and a modulation scheme. For example for a 10^{-3} BER and a 2-FSK non-coherent modulation scheme the required SNR is about 12.5 dB. The only parameter left is the noise bandwidth which ultimately affects the data rate. To meet the required ultra low power target, the transmitter node has to be duty cycled; it wakes up, it transmits the required data and it falls back in an ultra low power mode called idle mode. Let's consider P_{idle} the power consumption in the idle mode, P_{tx} the power radiated from the antenna including the power amplifier (PA) efficiency and P_{diss} the power used by the all circuitry before the PA. Then, the average power consumption of the transmitter node can be approximated by the following equation:

$$P_d = P_{tx}\frac{T_{tx}}{T} + P_{diss}\frac{(T_{tx}+T_{wu})}{T} + P_{idle}\frac{(T-T_{tx}-T_{wu})}{T} \quad (1)$$

where T_{tx} is the time required for each transmission, T_{wu} is the wake-up time of the transmitter (i.e. the time required to start up the circuitry and to acquire the synchronization) and T is the time interval between two consecutive transmissions. The duty cycle of the system, “d” can be defined as the ratio between the time required to transmit the data and the time between two consecutive transmissions. This time is the sum of the wake-up time, the transmission time and the time in which the transmitter is in the idle mode. The transmission time depends on the packet length L_{pack} and on the data rate “D”:

$$T_{tx} = \frac{L_{pack}}{D} \tag{2}$$

From these considerations, equation (1) can be re-written in the following way:

$$P_d = \left(P_{tx} + P_{diss}\right) \times d + P_{idle}\left(1 - d\right) + \left(P_{diss} - P_{idle}\right) \times d \frac{T_{wu}}{T_{tx}} \tag{3}$$

The required transmitted power is given by

$$P_{tx} = N_0 \times \frac{B_{noise}}{B_{data}} \times \frac{E_b}{N_0} \times NF \bullet D \bullet L \tag{4}$$

where E_b is the energy per bit of information, N_0 is the additive white Gaussian noise (AWGN) spectral density, B_{noise}[2] is the noise bandwidth

[2] The 2-FSK noise bandwidth can be approximated by the Carson rule as $B_{noise} = 2\left(\Delta f + f_m\right)$ where $f_m = \frac{2}{T_s}$ with T_s the symbol period and Δf the frequency deviation.

B_{data} [3] is the data bandwidth and "L_{path}"[4] are the path losses due to propagation. From equation (3), it can be seen that the power consumption can be reduced by reducing the duty cycle, the data-rate and by making the wake-up time small comparable to the transmission time. This last requirement becomes difficult to achieve in an FHSS system at high data rate due to pseudorandom-noise (PN) code synchronization.

Therefore, reducing the data rate will help relaxing the wake-up time for a given T_{wu}/T_{tx}. The transmitter average power consumption as a function of the data-rate for different duty-cycles is plotted in Figure 1. At high data rate the average power consumption is dominated by the transmitted power. At data rates below a threshold value the average power consumption is dominated by the pre-PA power. This threshold value depends on the pre-PA power dissipation and it is lower for lower values of the pre-PA power dissipation.

From Figure 1, when the pre-PA power dissipation is 2 mW this threshold value is around 100 kbps, while at pre-PA power of 10 mW it is located around 1Mbps. Furthermore, as expected at lower duty cycle the average power consumption decreases. At higher data rate, the wake-up time has to decrease considerably to keep the contribution to the average power consumption negligible. Synchronization times below 1 ms are not easily achievable. Therefore, from the previous analysis it is possible to conclude that a good strategy toward the reduction in the

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[3] For a 2-FSK modulated signal it equals four times the data rate.

[4] To calculate the path loss the following expression has been used: $L_{path} = 27.56 - 20\log_{10}(f_c) - 20\log_{10}(d_0) - 10 \bullet n \bullet \log_{10}\frac{d}{d_0}$ where f_c is the carrier frequency expressed in MHz, d is the communication distance in meters, d_0 the reference distance for free-space propagation (unobstructed transmission distance which is less than 2 or 3 meters in an indoor environment) in meters and n is the path-loss exponent.

average transmitter power consumption consists in reducing the data-rate and fastening the synchronization time for a given node duty-cycle.

5.1.System architecture trends

Different radio architectures have been recently studied in order to reduce the power consumption. Some of these architectures comprise Ultra-Wideband (UWB) transceivers, Super-Regenerative transceivers, Sub-sampling transceivers as well as Spread-Spectrum based transceivers (both Frequency Hopping and Direct Sequence (DS)).

5.1.1. Ultra wideband transceivers

Among different architectures suitable for an ultra-low power implementation, UWB based systems are gaining more and more attention. FCC rules specify UWB technology as any wireless transmission scheme that occupies more than 500 MHz of absolute bandwidth.

The most important characteristic of UWB systems is the capability to operate in the power-limited regime. In this regime, the channel capacity increases almost linearly with power, whereas at high SNR it increases only as the logarithm of the signal power as shown by the Shannon theorem

$$C = BW \times \log_2\left(1 + \frac{P_S}{P_N}\right) \tag{5}$$

where P_S is the average signal power at the receiver, P_N is the average noise power at the receiver and BW is the channel bandwidth. For low data-rate applications (small C), it can be seen from equation 5 that the required SNR can be very small given an available bandwidth in excess of several hundreds MHz. A small SNR translates in a small transmitted power and as a result in a reduction of the overall transmitter power consumption.

Although UWB transceivers can have reduced hardware complexity, they pose several

challenges in terms of power consumption. In Figure 2 a schematic block diagram of an UWB transceiver is shown. The biggest challenge in terms of power consumption is the analog-to-digital converter (ADC). If all the available bandwidth is used, the sampling rate has to be in the order of several Gsamples per second. Furthermore, the ADC should have a very wide dynamic range to resolve the wanted signal from the strong interferers. This implies the use of low-resolution full-flash converters. It can be proven [9] that a 4-bit, 15 GHz flash ADC can easily consume hundreds of milli-watts of power. Even if a 1-bit ADC at 2 Gsample/s is used, the predicted power consumption of the ADC remains around 5 mW [10]. Furthermore, the requirement on the clock generation circuitry can be very demanding in terms of jitter.

Besides these drawbacks, wideband low noise amplifier (LNA) and antenna design are challenging when the used bandwidth is in excess of some Gigahertz. The antenna gain, for example, should be proportional to the frequency [11], but most conventional antennas do not satisfy this requirement. LNA design appears quite challenging when looking at power consumption of state-of-the-art wideband LNAs [12]. A wideband LNA consumes between 9 and 30 mW making it very difficult to fulfill a constraint of maximum 10 mW peak power consumption for the overall transceiver. Nevertheless several successful designs are recently published showing the potential of UWB systems, their power consumption remains too high to be implemented in a "micro-Watt node". In [12] the total power consumption is around 136 mW at 100% duty cycle. In [13] a power consumption of 2 mW has been reported for the pulse generator only.

5.1.2. RF-ID, sub-sampling and super-regenerative architectures

In the wide arena of low-power architectures, RF-IDs represent a good solution when the applications scenario requires an asymmetric network. In this case the "micro-Watt node" needs

to transmit data and to receive only a wake-up signal. The required energy is harvested from the RF signal coming from the interrogator. In [14] the interrogator operates at the maximum output power of 4 W, while generating by inductive coupling 2.7 μW. This power allows a backscattering-based transponder to send OOK-modulated data back to the interrogator in a 12 meters range using the 2.4 GHz ISM band. Unfortunately the limited amount of intelligence at the transmitter side makes this architecture not flexible and only suitable in a highly asymmetric wireless scenario.

The Nyquist theorem has been explored in sub-sampling based receiver in order to reduce the overall power consumption. The power consumption of analog blocks mainly depends on the operating frequency. Applying the theory of band-pass sampling [15], it can be proven that the analog front-end can be considerably simplified reducing the operating frequency. This has the potential to lead to a very low power receiver implementation. Unfortunately due to the noise aliasing, it can be proven that the noise degradation in decibels is:

$$Dg = 10\log_{10}\left(1+\frac{2MN_P}{N_0}\right) \tag{6}$$

where M is the ratio between the carrier frequency and the sampling frequency, and N_p is the filtered version of N_0. In this sense, the choice of the band-pass filter BPF as well as the choice of the sampling frequency becomes quite critical. Beside this, the phase noise specification of the sampling oscillator becomes quite demanding. Indeed, the phase noise is amplified by M^2 requiring a careful design of the VCO. Consequently, when interferers are present, a poor phase noise characteristic can degrade the BER through reciprocal mixing considerably. Consequently, up to now, this architecture has been used mainly in interferer-free scenarios (space applications) [16].

Super-regenerative architectures date back to Armstrong, who invented the principle. Despite

many years of development, they still suffer from poor selectivity and lack of stability, while having the potential to be low power. Furthermore it is restricted to OOK modulation techniques only. In [17] bulk acoustic wave (BAW) resonators are used to reduce the power consumption and to provide selectivity. In spite of achieving an overall power consumption of 400 μW, it relies on non-standard technologies (BAW resonators), which will increase cost and form factor of the "micro-Watt node".

In [18] a 1.2 mW receiver has been designed and fabricated in 0.35-μm CMOS technology. Even though the power consumption is very close to the requirements of a "micro-Watt node", selectivity is quite poor. Indeed, to demodulate the wanted signal in the presence of a jamming tone placed 4 MHz far from the wanted channel with a BER of 0.1%, the jamming tone has to be no more than 12 dB higher than the desired signal. Generally, to achieve a reliable communication, the receiver should be able to handle interferers which have a power level 40 dB higher than the wanted signal with a BER smaller than 0.1%. This specification is very demanding for a super-regenerative architecture and it requires the use of non-standard components like BAW resonator to achieve a better selectivity.

5.2.Spread spectrum systems

Among the various competing SS techniques, the FH system, in which the transmitting carrier frequency is changing according to a prescribed PN sequence, offers an attractive solution in terms of hardware complexity, system performance and power consumption.

FH also enables the simplicity of using FSK modulation, which allows the possibility of employing a direct-conversion receiver architecture. In this way, a greater integration level and lower power consumption can be achieved. Furthermore, FSK modulation can be easily superimposed on the hopping carrier by simple digital techniques. Finally, the modulated output

has a constant envelope, and is amenable to non-linear power amplification. A schematic block diagram of an FH transmitter is depicted in Figure 3(a), while the distribution of the signal in the time-frequency plane is depicted in Figure 3(b).

5.2.1. DSSS vs. FHSS

Differently from a DSSS system, in an FHSS system the spreading code is applied on the carrier frequency rather than on the modulated data. This choice has some advantages as well as some drawbacks. In terms of power consumption, the wake-up time required by the system will be considerably lower. The wake-up time takes into account also the synchronization time. It can be proven that the average acquisition time for an SS system is

$$\overline{T_{sync}} = \left(N_{cell} - 1\right) T_{da} \left(\frac{2 - P_d}{2 P_d} \right) + \frac{T_i}{P_d} \tag{7}$$

where T_i is the integration time for the evaluation of each cell in the time-frequency plane, P_d is the probability of detection when the correct cell is being evaluated, T_{da} is the average dwell time at an incorrect phase cell, and Ncell is the total number of cells. Now, assuming that no frequency uncertainty is present, there will be a time misalignment between the two PN sequences at the transmitter and receiver side equal to ΔT_i. Therefore, while for a DSSS the system has to be synchronized within $T_C/2$ where T_C is the chip duration, an FHSS system needs to be synchronized within $T_s/2$. Due to the fact that in a DSSS system the processing gain is related to the ratio between the chip rate and the symbol rate, the chip period is at least an order of magnitude smaller than the symbol period. As a result, the number of cells that have to be evaluated in a DSSS system is considerably bigger than in an FHSS system. From equation 7 the mean DSSS synchronization time is bigger than in the case of an FHSS system. This will increase the wake-up time and therefore the overall system power consumption.

SS systems are generally affected by the so called near-far problem. The near-far problem is the

major limitation in DSSS systems and increases the complexity of the transceiver due to the need for power control circuitry. Without any power control, the performances of a DSSS system in an environment in which other DSSS systems are present can be heavily spoiled. As shown in Figure 4, in an FHSS system (Figure 4(a)), when User1 is 5 times further away from the receiver compared to User2, the BER is still below 5%. At the same relative distance, the DSSS system (Figure 4(b)) has already a BER of about 50%. The results shown in these plots have been obtained using Simulink® models, in which the users were interfering continuously with each other and only an AWGN channel has been considered. In reality, the probability that two or more users will communicate simultaneously, is in the order of a few percent. Consequently, the average bit error rate should be scaled down accordingly. In conclusion, there is a high probability that in a DSSS system an Automatic Gain Control (AGC) should be used while, in an FHSS system, it can be easily avoided, reducing the complexity and the power consumption of the system.

Unfortunately, the requirements on the hopping synthesizer in terms of settling time and accuracy in the frequency synthesis are quite stringent. Therefore, the implementation of FHSS functionalities in a "micro-Watt node" requires a novel simplified architecture with power consumption an order of magnitude smaller than the state-of-the-art.

6. Frequency Hopping Spread Spectrum Synthesizers

The main challenges in the implementation of an FHSS system result from the requirements for agile and accurate frequency hopping at very low power levels. Several ways to generate the hopping bins have been proposed in the recent years. Whereas widely used also for high data-rate links, fractional-N [19] and Direct-Digital Frequency Synthesizers (DDFS) [20] based synthesizers are relatively power hungry. In [19] the synthesizer power consumption is 55 mW

from a 2.5 V power supply while in [20] the synthesizer dissipates 40 mW from a 3 V power supply.

Fractional-N based synthesizers have to deal with increased phase noise coming from the Σ-Δ modulator. Indeed, the quantization noise is filtered by the PLL phase transfer function and converted into phase noise [21]. Concluding, a trade-off between phase noise and settling time exists. Phase noise can increase the system BER by reciprocal mixing. Therefore, it should be kept low by increasing the reference frequency or the order of the loop filter [22]. This will increase in both cases the overall power consumption.

Recently, a new system concept has been proposed based on Analog-Double Quadrature Sampling (A-DQS) to relax the specifications on the synthesizer [23]. The channel selection originally performed by the synthesizer can be partitioned to the A-DQS. In this way, the step size of the PLL synthesizer can be doubled and the locking position of the LO in the entire frequency band is halved. Nevertheless, the power consumption remains too high, mainly due to the ADC requirements [24].

In a DDFS, a sine-wave is synthesized in the digital domain through the use of a simple accumulator, which produces, as an output, a ramp proportional to the desired frequency, and a phase-to-sine amplitude converter. In the simplest case this converter is a Read-Only Memory (ROM). A digital-to-analog converter (DAC) and a Low-Pass Filter (LPF) are used to convert the sinusoid samples into an analog waveform.

The main operation in a phase accumulator of N-bit length is the N-bit addition. From [25] the energy required for an addition by an Arithmetic and Logical Unit (ALU) can be considered in the range of 300 pJ per addition (16-bit addition). If a bandwidth of 9.6 MHz (64 channels spaced by 150 kHz in the 915 MHz ISM band) should be synthesized using the architecture

proposed in [20], then a 25 MHz reference clock is needed and the power consumption of the phase accumulator can be predicted by the following equation:

$$P_{phase-acc} = f_{ref-clk} \times E_{add} \tag{8}$$

where $f_{ref\text{-}clk}$ is the reference clock frequency and E_{add} is the energy per N-bit addition (300 pJ). From Equation 8 the predicted power consumption for the phase accumulator is 7.5 mW. The second block in a DDFS, which to a great extent has significant power consumption, is the ROM.

Generally, even if a resolution of few Hertz is needed to keep the spurious level low, practical words longer than 14 bits will lead to a very large ROM even if compression techniques are employed. Considering a truncated 14-bit phase word and a 12-bit word length for the amplitude mapping, then the size of the ROM will be approximately 192 kbit. Splitting, for convenience, the ROM in three banks of approximately 64 kbit, then it can be implemented by three $2^8 \times 2^8$ matrices.

Defining the storage array as a $2^n=2^{n-k}\times 2^k$ matrix with 2^n memory cells, 2^{n-k} rows and 2^k columns, then from [26] most of the power consumption in a ROM comes from the pre-charge or the evaluation of the 2^k memory cells. Therefore, we can approximate the total power consumption by the following:

$$P_{mem-cell} = 3\frac{2^k}{2}\left(c_{\text{int}} l_{column} + 2^{n-k} C_{tr}\right) V_{dd} V_{swing} \tag{9}$$

where $P_{mem\text{-}cell}$ is the approximated power consumption of the ROM, the factor 3 takes into account that the total memory required has been split into three ROMs of smaller size, c_{int} is the capacitance of a unit wire length with minimum width, C_{tr} is the minimum size gate capacitance, V_{dd} is the power supply voltage and V_{swing} is the voltage swing of each memory cell.

Defining the memory cell as $d_m \times d_m$ square, then the column interconnection length of the

memory matrix is $l_{column}=2^{n-k}d_m$.

Now, considering as an example the CMOS 0.18 μm technology, a 5.4 mW predicted power consumption for the ROM is obtained. As a result, the peak power consumption of the DDFS excluding DACs is higher than the 10 mW limit of a "micro-Watt node".

6.1.Pre-distortion-based hopping frequency synthesizers

A conceptual block diagram of the proposed architecture is depicted in Figure 5. The incoming data, together with the wanted hopping code, addresses a particular word cell in the ROM. The ROM has been split into two blocks depending on the modulation bit. In each memory cell the pre-distorted word that will drive the DAC with a defined data bit is stored. The DAC then drives directly the varactor array changing the capacitance and therefore the VCO oscillation frequency according to the desired frequency bin and data.

The frequency of an LC type oscillator and the tank capacitance are related by the following well known relation

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{10}$$

where L and C are respectively the total capacitance and inductance of the tank and f_{osc} is the oscillation frequency. This, in practice, is realized by using a varactor diode, which has a capacitance that varies non-linearly with its reverse voltage. Therefore, by applying the correct voltages to the varactor diodes, it is possible to synthesize all the required frequency bins with minimum hardware complexity (virtually only a VCO).

In an FHSS system the various frequency bins are addressed in a pseudo-random fashion. Pseudo-random codes are generated in the digital domain, while the varactor diodes require an analog control voltage. Consequently, a DAC is required as interface between the digital world

and the analog world. While passing from the digital world to the analog world several non idealities can affect the precision with which the frequency bins are generated. The main sources of error in this conversion process are the following:

- DAC quantization error (deterministic)
- Varactor non-linearity (deterministic and stochastic)
- DAC INL (stochastic)
- Square-root relation between frequency and tank capacitance (deterministic)

All these non-idealities in the transmitter chain can be divided in two groups. One group has a deterministic behavior and it does not vary due to process spread. In this category falls the square-root non linear relation and the DAC quantization error. The other group has a stochastic behavior. This means that it will depend on the process spread and therefore a different behavior can be expected for different ICs.

6.1.1. Deterministic errors

The non-linear relation between frequency and tank capacitance can be easily corrected by mapping the required frequencies in required capacitance values. From these values, knowing the varactor characteristic, to a set of required voltages and knowing the DAC specifications to a set of digital words, which can be stored in a ROM.

Therefore, neglecting for the moment the stochastic nature of the DAC linearity and of the C-V characteristic of the varactor, the problem simplifies in correctly choose the DAC resolution to reduce the residual frequency error below a certain threshold.

The quantization error, will produce a non-linear frequency error passing through the non-linear

C-V characteristic of the varactor and through the square-root relation between frequency and tank capacitance.

Looking at the square-root relation, when the overall capacitance is the smallest (at higher frequencies), an error on the capacitance due to quantization, will produce the largest error in the synthesized frequency. In this situation, the reverse voltage applied to the varactor is at its maximum value (for example -1.6 V). In this region, the varactor exhibits a highly linear behavior, contributing less to the overall frequency error. In this conditions, the frequency error is mainly caused by the quantization error passing through the square-root relation.

Close to the minimum reverse voltage (for example -0.2 V), the varactor characteristic is highly non-linear. In this case the frequency error is mainly caused by the quantization error passing through the varactor non-linearity, while the square-root relation will minimally contribute to it.

In both cases a maximum capacitance error can be defined above which a frequency error larger than the required threshold is present at least in one of the synthesized frequency bins. These maximum errors are in the two cases ($\Delta C_{\sqrt{LC}}$ and ΔC_{var}) defined as follows

$$\Delta C_{\sqrt{LC}} = \frac{1}{\left[2\pi\left(f_{max} + \Delta f\right)\right]^2 L} - C_{min} \tag{11}$$

$$\Delta C_{var} = \frac{1}{\left[2\pi\left(f_{min} - \Delta f\right)\right]^2 L} - C_{max} \tag{12}$$

where f_{max} is the highest channel center frequency, f_{min} is the lowest channel center frequency, Δf is the maximum allowed frequency offset, C_{min} is the capacitance at the highest channel frequency, C_{max} is the capacitance at the lowest channel frequency and L is the LC-tank inductance value.

The maximum acceptable frequency error after pre-distortion can be derived by the following considerations. PN-codes orthogonality has to be preserved. This means that the relative position

of the channels along the frequency grid has to remain unchanged with respect to the ideal case. From this consideration, a maximum frequency error equal to the inter-channel spacing is allowed (for example 100 kHz). If a 100 kHz maximum channel frequency shift is considered, then there would be the possibility that two channel gets adjacent to each other (the inter-channel spacing becomes zero). In this situation, if the specification on the oscillator phase noise remains unchanged, the amount of noise leaking in the adjacent channels increases degrading the SNR in those channels.

In order not to degrade the BER in the adjacent channels considerably, a 0.5 dB maximum degradation on the phase noise has been considered[5].

Under this condition, a maximum uncorrected frequency error of 25 kHz can be tolerated [27]. Considering a 1.4 V swing on the varactor control voltage, an inductance value of 4.1 nH, and 64 channels placed around 915 MHz (ISM band), it can be found from equations (11, 12) that the largest error comes from the quantization error passing through the varactor non linear C-V characteristic. This is shown in Figure 6. In this picture three curves are represented. The two solid lines curves represent the calculated (via equations 11 and 12) and simulated maximum residual frequency error after pre-distortion is applied versus the DAC resolution. In this example the DAC is considered linear (INL=0). The dotted line curve represents the position in the frequency range at which the aforementioned frequency error occurs. As can be seen the largest frequency error due to the quantization error occurs at the lower portion of the frequency

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[5] The error probability of a non-coherent BFSK modulated signal is given by $\frac{1}{2}e^{-\frac{E_b}{2N_0}}$. Considering a 0.1% initial BER, a 0.5 dB degradation in the phase noise translates in a 0.5 dB degradation in the SNR at the demodulator input and therefore in a BER close to 0.2%.

range[6] .

From the previous discussion it has become evident that the quantization error translates in a non linear frequency error by passing through the varactor C-V curve and through the square root relation. It has been shown that in the lower portion of the frequency band the frequency error mainly depends on the effect of the varactor non-linearity on the quantization error while in the upper portion of the frequency band the square root function has the dominant effect. Looking now at Figure 6, in which both the non-linearities are considered, it can be concluded that the frequency error coming from the DAC quantization error is mainly caused by the non-linear mapping of this error in the frequency domain via the C-V characteristic of the varactor.

Given that the maximum residual frequency error has to be lower than 25 kHz, from Figure 6 it can be concluded that a 10 bit DAC is sufficient to achieve the required specification.

6.1.2. Stochastic errors

In the previous analysis the DAC has been considered linear and the spread on the varactor capacitance has been neglected. In the real case they will affect the overall residual frequency error.

Given a certain DAC, its non-linear behavior can be taken into account by applying a dedicated pre-distortion table. Unfortunately, the INL of each DAC will be different due to its statistical behavior. Therefore, this would require a different programmable look-up table per chip, which would be too costly for a system that aims to be very cheap. As a result, it is necessary to fulfill

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[6] Given 64 channels and a 150 kHz separation between adjacent channels, the minimum and maximum channel frequencies are 910.35 MHz and 919.65 MHz respectively.

the required specifications on the residual frequency error even when the DAC statistical properties do change.

A DAC model has been built in Simulink, which includes also its non-linear behavior [27]. The results are shown in Figure 7. Here both the quantization and the INL of the DAC are considered. Roughly four regions can be recognized. The upper region (*Out of spec*) does not fulfill the maximum residual frequency offset requirement. Then there are two regions namely *Difficult* and *Not worth*. The first region presents a difficult task for the designer due to harsh requirements in terms of maximum INL. The second one, while relaxing the INL requirements, necessitates the design of a higher resolution DAC than in the *Useful area* to fulfill the maximum residual frequency error specification. Designing one more bit of resolution generally requires more area and more power. So the design of the DAC is near optimum inside the *Useful area* in Figure 7.

Indeed, in this region the INL requirements are not too harsh and the residual frequency error due to the combined effect of both quantization error and DAC INL is smaller than the 25 kHz specification. This region is divided in two by the bold line. This line represents the points at which the contribution of the quantization error and of the INL to the residual maximum frequency error are equal. Therefore, the right part of this area is dominated by the INL error while the left part by the quantization error. Reducing the number of bits will reduce the chip area and in the end the costs and the power consumption of the DAC. As a result, given the low frequency operation of the DAC, a lower resolution DAC, which does not require an extremely small INL can be chosen.

Among different DAC specifications which fulfill the maximum residual frequency error requirement, given the previous considerations and looking at Figure 7, a 10-bit DAC with an

INL between 1 and 1.5 mV can be chosen as a near optimum solution.

The last source of error is the variation in the C-V characteristic of the varactor due to the process spread. As for the DAC INL, this problem can be corrected by a dedicated pre-distortion look-up table. Though this is an effective solution it can be costly.

Figure 8 shows the measured fine tuning range of 20 IC samples, each calibrated to a common center frequency (915 MHz) via coarse tuning (namely f_c in Figure 12(a) and Figure 12(b)). The channel bin tuning voltages are generated by the DAC, driven by the base-band microprocessor. The look-up table in the ROM has not been changed and also the DAC is the same, therefore the final effect is only due to the process spread on the varactor. Although the maximum frequency deviation of 20 ICs within the same batch were found to be no more than 220 kHz ($\sigma \approx 32$ kHz), inter-batch spreads will be larger.

In Figure 9(a) the two extreme cases in Figure 8 are plotted. The effect of the varactor spread (in the two aforementioned extreme cases) on the position in the band of the frequency bins for a given pre-distortion table is illustrated in Figure 9(b). It can be seen that due to the difference in the varactor C-V characteristic, there is a frequency offset accumulating while moving from channel 1 to channel 32 or from channel -1 to channel -32. The maximum error is present at the channels ±32 as can be seen also from the measured curves in Figure 8. Given the monotonicity of the C-V varactor characteristic the amount of frequency error due to the different C-V characteristic between two adjacent channels is negligible compared with the frequency error due to the quantization error. Unfortunately if the pre-distortion table is kept the same for all the ICs in a batch, these phenomena will pose problem at the receiver side. Due to its statistical dependence from the process, the absolute position of the last channel with respect to the ideal position will be known with a precision of ±110 kHz(see Figure 8). All the other channel

positions will be known with a precision better than that.

Therefore, at the receiver side the channel bandwidth has to be as large has 370 kHz while the inter-channel spacing larger than 185 kHz. This is clearly shown in Figure 10. Indeed the absolute position of the channel can spread 110 kHz (at 4σ) in both direction. Furthermore the quantization error plus the INL of the DAC will add in the worst case 25 kHz more uncertainty in the channel position. Finally the two channels should not overlap in the two worst case and therefore the center frequency of the adjacent channel has to be at least the bandwidth apart (in this case 50 kHz). Therefore, the baseband filter has to span two times 185 kHz which makes 370 kHz.

If all the 64 channels are utilized, than the occupied bandwidth will be around 12 MHz. Given that no crystal has to be used, then this will pose some more strict requirements on the reference frequency accuracy. Indeed the accuracy has to become better than 0.75% in this case, while in the implemented case can be relaxed to 1 %. On the other hand, FCC rules demand for only 25 hopping channels for power levels below 0.25W (which is generally the case for ultra-low power wireless nodes). Therefore another possibility is to still keep the 1 % accuracy for the reference frequency but reducing the number of hopping channels.

6.1.3. Data recovery

FSK modulation is very sensitive to frequency offsets. For example in a correlator type demodulator the frequency offset has to be much smaller than the data rate for a BER lower than 1 %. If a 1 kbps data rate is chosen than the residual offset has to be no more than few hundred hertz. Looking at Figure 6 and Figure 7 it can be seen that a DAC with more than 14 bits is

needed for a reasonable INL requirement.

Furthermore, a technological solution or a calibration circuitry would be needed at the transmitter side in order to correct for the statistical variation of the C-V varactor curve. Therefore, the choice of the demodulator at the receiver side is crucial in order to reduce the complexity at the transmitter side.

In [28] several demodulator topologies have been studied, with respect to their performances, in the presence of static frequency errors (these errors are caused by the statistical properties of the DAC and of the varactor and therefore are time invariant in first approximation). The Short-Time DFT (ST-DFT) algorithm, through differential encoding, shows a remarkable immunity against static frequency offsets. Furthermore it can be applied in the digital domain which has the potential to be low power. Indeed, if a zero-IF architecture is employed, due to the small signal bandwidth, the operating frequency of the ADC will be around 200 ksample/s at the Nyquist rate (signal bandwidth equal to 50 kHz).

As shown in [29], the capability of the ST-DFT algorithm to reject the frequency offset depends upon the condition that the offset is slowly varying. In other words, the frequency offset should vary at a rate smaller than the data-rate. Therefore, the offset between two consecutive bits can be considered the same and it will be canceled out when differential encoding is applied. In this way also the frequency error due to temperature and power supply variations can be tracked and actively canceled out without requiring any additional circuitry.

While differential encoding can cancel out, when applied to two consecutive bits, frequency errors induced by temperature or power supply variations, it cannot cancel the frequency error induced by the statistical properties of the DAC and of the C-V varactor characteristic. Indeed, in the particular case of the proposed FHSS system, each bit is sent on a different channel, which

is affected by a different offset due to the INL distribution of the DAC as well as the varactor C-V characteristic spread.

This means that two different bits will have two different offsets and, therefore, the simple differential encoding cannot cancel it out. Therefore a straightforward way to cope with such a problem is to use again a dedicated look-up table for each IC. Though this approach guarantees an easy solution to the previous problem, it will increase the cost of the final wireless node due to an increase in testing and calibration costs.

Another solution is to send at the beginning of each hopping information about the offset present at that particular hopping frequency. The principle is depicted in Figure 11. In the figure the offset is sent as a high logic level but it can be chosen to be a low logic level as well. Due to the fact that the offset and the data are sent now on the same frequency bin, they are both affected by the same frequency error (due to the statistical properties of the DAC INL and the C-V characteristic of the varactor). The differential encoding, therefore, can provide in this case the final cancellation. The drawback of such a solution is an increase in the data rate. Given the large modulation index employed (m>5) and the low data-rate there will be no severe drawback at the receiver side. Therefore, this technique has been chosen for the proposed implementation.

7. FHSS Pre-distortion Based Transmitter Design

Two different transmitter RF front-ends have been realized in bipolar Silicon-on-Anything (SOA) technology. The front-end has to be as simple as possible while pushing the complexity in the digital domain. This is achieved by using the pre-distortion technique previously described. All the digital words stored in the ROM (see Figure 5) are calculated so that they take into account the DAC quantization error and its effect via a non-linear transfer function (square root

and varactor) on the frequency error. The INL of the DAC has to be compensated separately for each IC or can be left uncompensated if it is smaller then 1.5 LSB for a 10-bit DAC (see Figure 7). The two architectures are depicted in Figure 12.

In Figure 12(a) a common oscillator-divider front-end is shown. The system front-end consists of a resonator based LC-VCO, a divider and an output stage able to deliver -25 dBm power on a 50 Ω load. To minimize oscillator pulling the VCO operates at 1.8 GHz and is divided down to the TX frequency. V_{fc} is the coarse control voltage and it is used to calibrate the hopping channels inside the ISM band. The second divider, connected to a second buffer, is used inside a frequency locked loop (FLL) loop for the initial center frequency calibration. Once this calibration is performed, the FLL and related dividers are powered down, thus not contributing to the total power dissipation. V_{ff} is the fine control voltage and it is used to synthesize the 64 channel frequencies. The FHSS control, which is realized in baseband, generates the PN hopping code, and it outputs the N-bits pre-distorted digital words. These words are applied to the DAC to synthesize the required control voltage for the fine varactor bank.

Figure 12(b) shows a single building block RF front-end. It is a combination of VCO and a PA, of which the coarse frequency calibration code can be factory set and stored in an EPROM. This code will be converted into an analog voltage by a DAC. The output of the DAC will directly drive the coarse varactor on the power-VCO. The synthesis of the channel frequencies is obtained in the same way as for the architecture shown in Figure 12(a). In this case, the oscillator center frequency is at 915 MHz instead of 1.83 GHz, which can reduce the system power consumption. Furthermore, no PA is required, but the VCO is directly coupled to the antenna through a balun.

The baseband part has been implemented using discrete components for both architectures. The

microprocessor is a PIC18F627A, which consumes 12 μA at 32 kHz, while the DAC is an AD7392 [30], which draws 100 μA. The transistor level schematics of the two front-ends are depicted in Figure 13.

The divider in Figure 13(a) is a traveling wave divider. In this design the often present external base-resistors of the upper stage are not used and the design is optimized by proper transistor dimensioning to have maximum divider sensitivity at 1.8 GHz and low power dissipation (200 μA). The output buffer (not shown) is a differential pair (2 mA). The oscillator core consumes 550 μA while achieving a -109 dBc/Hz phase noise at 450 kHz from the carrier.

The second architecture (Figure 13(b)) consists only of a directly modulated RF cascoded Colpitts power VCO. Cross-coupled oscillators (Figure 13(a)) have been preferred over other topologies for monolithic integrated circuit implementation because they are easily realized using CMOS technology and differential circuitry. Due to the use of the tail current source, cross-coupled oscillator topologies present phase noise performances worse than classical types of oscillator with one of the active device ports grounded. In addition, classical type of oscillator topologies provide larger oscillation amplitudes for a given bias current because there is no voltage drop of the DC current across the current source element enabling, in this way, optimization of the power consumption.

One of these configurations is based on the Colpitts topology. Isolation problems can degrade VCO performances in terms of phase noise and frequency stability through phenomena like VCO pulling. This problem arises from changes in the load conditions, and therefore requires a buffer stage between the VCO and the output stage, which will increase the overall power consumption. To minimize the power consumption, the VCO and its buffer are connected in series to reuse the bias current between the two stages. For these reasons, a common collector

Colpitts oscillator has been chosen together with a common base buffer stage, arranged in a cascode configuration.

In this way, the current consumption is minimized, pulling is reduced due to better isolation between the tank and the load and no PA is required, instead the cascode stage can directly drive the antenna through a balun. As a result, a single block RF front-end is obtained. A differential configuration has been chosen to reduce the second order harmonic distortion term, which can degrade performances at the receiver side in a zero-IF architecture.

The bias current level largely depends on the required output power levels. It is desirable that phase noise requirements are met over a wide output power range. The output power can then be controlled by changing the bias current while meeting the BER specifications over the entire control range.

7.1.Experimental Results

The two RF frond-end ICs are shown in Figure 14(a) and Figure 14(b). The FE1 front-end occupies 2.8 mm^2 while the FE2 front-end 3.6 mm^2. Figure 15 shows the required bias current for the power VCO versus the output power and phase noise performance at 450 kHz far from the carrier for the front-end in Figure 14(b). The required bias current ranges approximately between 1 and 2 mA to obtain an output power between -18 dBm and -5 dBm. Simulated and measured results show a good agreement allowing minimization of the current consumption for a given set of output power and phase noise specifications. Indeed, in Figure 15 the phase noise varies between -102 dBc/Hz and -115 dBc/Hz when the bias current changes between 1 and 2 mA, which is better than the required specification of -100 dBc/Hz at 450 kHz from the carrier.

In Figure 16 the whole chain, from the look-up table in the microprocessor up to the evenly spaced FH spectrum is shown. In the measurement results shown in Figure 16, the 64 channels

are addressed sequentially rather than in a pseudorandom fashion. As can be seen, the output of the DAC has a non-linear shape in time due to the pre-distortion algorithm. Moreover, the channels are equally spaced with a maximum frequency error smaller than 5 kHz. This frequency error is smaller than theoretically predicted, due to the higher DAC resolution. Indeed, a 12-bit DAC has been used even if a 10-bit DAC was sufficient as explained in Section 6.1.

To demonstrate a reliable wireless link at the specified output power levels and phase noise specifications and to prove the pre-distortion concept, a FH transmitter has been realized. Two isotropic antennas placed 8 meters apart were used in a Non-Line-of-Sight (NLOS) configuration in a normal office environment.

The transmitted power has been set to -25 dBm while the receiver employs a ST-DFT demodulation algorithm and a super-heterodyne architecture. The measured received power is on average -75 dBm. In this condition, the measured raw BER is lower than 1.1% at 1 kbps data rate and 1 khop/s hopping rate. The overall measured transmitter power consumption is 2.4 mW (for the front-end in Figure 14(b) at 100% duty-cycle) from a 2 V power supply and 5.4 mW (including the buffer) for the front-end in Figure 14(a) from 1.8 V power supply. The baseband and mixed signal circuitry including the DSP dissipate 0.4 mW mostly consumed in the DACs[7].

In Figure 17 the received spectrum before demodulation (Figure 17(a)) is shown together with a summary of the performances of the realized front-ends (Figure 17(b)).

8. Receiver Planning

A receiver front-end needs to achieve different objectives: amplification, mixing, filtering and

[7] The baseband power consumption can be reduced to 0.2 mW if the coarse calibration DAC is switched off after coarse calibration is achieved.

demodulation. For “micro-Watt” nodes, given the low mobility of the wireless nodes and the small channel bandwidth, a slow fading condition is foreseen. Thus, diversity and equalization are not needed, simplifying, in this way, the demodulator.

8.1.Receiver architecture

The transceiver architecture impacts complexity, cost, power dissipation and the number of external components. Two very common architectures are generally used in integrated transceivers: heterodyne and homodyne. In heterodyne architecture, the signal is down-converted to a lower IF frequency to relax the required Q needed at high frequencies to filter a narrowband signal from large interferers. Figure 18 shows a simplified block diagram of a heterodyne receiver.

The principal consideration in this architecture is the image frequency. This issues can be easily understood noting that all the signals at a distance equal to ω_{IF} from the LO frequency will be down-converted to the same IF frequency. This is illustrated in Figure 19. To suppress the image frequency, an image reject mixer is often used. The choice of the IF is not trivial and it entails a trade-off between sensitivity and selectivity. Generally the image reject mixer is realized using external components. This translates in a worst transceiver form factor and it requires the LNA to drive a 50Ω impedance. This finally translates in higher power consumption due to a larger required current.

The simplicity of the homodyne architectures makes this topology very attractive for ultra-low power transceiver. The RF signal is directly down-converted to baseband. Figure 20 shows a simple homodyne receiver. In the general case of phase or frequency modulated signals, the information at positive and negative frequencies of the spectrum is different. Therefore, this topology requires quadrature down-conversion. Nevertheless, the homodyne receiver offers two

big advantages over the heterodyne architecture. First no image rejection filter is required, second the often external IF filter is replaced by two simple LPF, which can be easily integrated. Unfortunately, homodyne receivers suffer from I/Q mismatch, even-order distortion, DC offset and flicker noise. Flicker noise and DC offset can be overcome for low data-rate application by employing wideband FSK modulation followed by a high-pass filter which can be sometimes a simple AC coupling capacitance. This techniques solves also partially the even-distortion problem in the case the received signal contains some amplitude modulation. Indeed, if the information is carried by the frequency, the received signal can be hard-limited cancelling any unwanted amplitude modulation. I/Q mismatch can be reduced by proper layout and matching techniques.

Given the aforementioned consideration, the proposed architecture is a zero-IF topology and is depicted in Figure 21.

8.2.A 2.4 GHz receiver link budget analysis

Any channel and demodulator impose some boundary conditions on the RF front-end. These conditions can be specified in terms of SNR and can be translated to circuit concepts like NF, gain and distortion. Next it is necessary to translate these boundary conditions in to boundary conditions of the front-end sub-blocks.

8.2.1. Propagation-link budget analysis

The first step consists in calculating the minimum received signal known as receiver sensitivity. The received signal P_{RX} can be expressed in terms of transmitted power P_{TX} and channel losses L_{path} by Equation 14.

$$P_{RX} = P_{TX} - L_{path} \tag{14}$$

The losses in the channel can be expressed by the following equations [31].

$$L_{path,LOS} = -27.56dB + 20\log_{10} f_c + 20\log_{10} d_0 \quad (15)$$

$$L_{path} = L_{path,LOS} + 10 \bullet n \bullet \log_{10} \frac{d}{d_0} \quad (16)$$

where f_c is the carrier frequency expressed in MHz, n is the path loss exponent, which indicates how fast the path loss increases with distance, d_0 is the reference distance in meters for free-space (unobstructed) propagation, $L_{path,LOS}$ is the corresponding propagation loss of the line of sight (LOS) path, and d is the distance in meters between transmitter and receiver[8]. Considering a three meters reference distance, a -6 dBm transmitted power and a maximum communication distance of 30 meters with n=3 the receiver sensitivity is about -85.6 dBm in the 2400 MHz ISM band.

The required SNR at the demodulator input largely depends on fading conditions. When a BFSK modulation technique is used, it can be proven that the required SNR is [31]

$$\Gamma = \frac{E_b}{N_0}\overline{\alpha^2} \quad (17)$$

where α is the gain of the channel with Rayleigh distribution. The term Γ represents, indeed, the average value of the normalized SNR. The error probability, for non-coherent BFSK modulation, is then given by [31]

$$P_{e,NCFSK} = \frac{1}{2+\Gamma} \quad (18)$$

For a 1% BER the required SNR is 20 dB. Furthermore, this already large SNR has to be met also when interferences are present. Because these interferences are random in nature, the demodulator cannot differentiate them from the channel noise and will process them during the

[8] Isotropic antennas have been assumed at both the receiver and the transmitter sides. Indeed, in a sensor network

demodulation operation. In such situation the SNR is reduced even more.

8.2.2. Link budget analysis of discrete parts

The first step is to filter out the noise and the interferences which are out of the band of interest. This is accomplished by the BPF in Figure 21. The quality factor of this filter is generally quite high. For the band of interest the required Q has to be 2400/83.5≈29. It is generally realized as an external LC network, but this approach increases the form factor and the cost of the wireless node. Therefore the integration of the BPF filter is highly desirable.

Several ways can be used in the design of integrated BPF filter. One possibility consists in using integrated passive components to realize the common LC ladder of a BPF filter. Unfortunately, on-chip inductors have very poor Q limiting de facto the Q of the entire filter. The Q is related to the losses in the inductive element of the filters and therefore, can be made very large if the losses are reduced. One way to accomplish this result is to use on-chip transformers [32]. The unloaded filter Q is given by

$$Q_{unloaded} \approx Q_{inductor} \frac{1+k}{1-\beta k} \tag{19}$$

where k is the coupling factor and β takes into account losses in the transformer. Equation (19) shows that small increase of k leads to a significant increase of the filter unloaded quality factor. Starting from a $Q_{inductor}$≈2 a filter Q of about 10 has been achieved. To increase the unloaded Q of the filter an active topology is needed [33]. Unfortunately, though a Q≈3000 is achieved, the required active components (CMOS transistors) consume around 10 mW while achieving 3.1 dB gain. Consequently, this topology cannot be used for ultra-low power applications.

The last possibility relays on using FBAR resonators. Their size is between 5 and 8 times smaller

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there is not, in general, a LOS condition and therefore isotropic antennas must be used.

then surface acoustic wave (SAW) based filters. A 1.9 GHz FBAR BPF filter has been realized in [34]. The total required volume is 1.0 mm × 1.0 mm × 0.7 mm. An insertion loss of 3.3 dB has been measured with 35 dB rejection in the upper stop-band and 25 dB in the lower stop-band.

Concluding, the two most promising way to achieve integration of the BPF filter are the one based on on-chip transformers and the one based on FBAR resonators. Nevertheless, the Q of the first topology is still below the receiver specifications while the second one cannot be still considered fully integrate. Therefore, there is a large margin of improvement in this field for researchers.

In this work, passive structures will be used for the BPF the balun and the TX-RX switch. The only required specification is the attenuation, which is then taken from available components off the shelf.

8.2.3. Link budget analysis for integrated parts

The receiver chain has to assure a certain SNR at the demodulator input. This SNR has been previously evaluated around 20 dB when worst case fading is considered for a 1% BER. For noise calculation the noise bandwidth needs to be calculated. The noise bandwidth is the smallest bandwidth in the receiver chain and it strongly depends on the channel bandwidth. Considering a 2kbps data-rate and a modulation index equal to 5, from the Carson's rule a 24 kHz signal bandwidth is required. Increasing the data rate will increase the bandwidth and, therefore will reduce the available receiver NF. If the bandwidth has to remain the same in order to relax the receiver requirements, then the modulation index has to be reduced. This will make the effect of flicker noise and DC offset more severe. Therefore the data-rate can be increased by a combination of a smaller modulation index and larger signal bandwidth.

If a 24 kHz bandwidth is considered, then the specification on the Anti-Aliasing (AA) filter will

become prohibitive. This means that generally a certain over-sampling ratio is needed at the ADC side in order to relax the AA filter specifications. In this case an over-sampling ratio of four has been considered. The choice of an over-sampling ratio, though it appears spoiling the SNR by enlarging the noise bandwidth, will not have, in reality, any counterproductive effect. Indeed at the DSP side, the SNR will improve, through decimation, by a factor roughly equal to the over-sampling ratio. For the moment a Nyquist bandwidth of 96 kHz will be considered for noise calculations.

In Figure 22 the specifications for each block have been derived. While it appears that no LNA is present, in reality it is merged with the mixer. To meet the low power target, the simple cascaded LNA-mixer topology is not efficient. It requires two current sources while achieving a voltage gain and a NF which are too close to the required specifications. In [35] the LNA-mixer front-end consumes 3.6 mA while achieving a 21.4 dB voltage gain and 13.9 dB of NF. For low-power applications LNA and mixer should be merged in a single block, reusing the current. Following this approach in [36] a current reused LNA-mixer front-end with 31.5 dB voltage gain and 8.5 dB NF at 500 μA current consumption (1.0 V power supply) in 0.18-μm technology has been recently proven. Comparing these figures with the specifications in Figure 22, it clearly appears that there is still room for a further reduction in the current consumption. The signal and the noise level along the receiver chain are depicted in Figure 23(a).

While in principle the ADC can be replaced by a limiter (1-bit ADC), in reality this choice poses some drawbacks. Any radio system has to work in an environment full of other radios using the same propagation medium (the air) potentially interfering each other. Therefore, every radio must have a certain dynamic selectivity to cope with this scenario. Considering a simple 2^{nd} order Butterworth filter as an AA-filter, the signal and blockers level throughout the chain are

depicted in Figure 24. As can be seen, only around 10 dB Carrier-to-Interferer (C/I) ratio is achieved in the adjacent channel while for the alternate and third and beyond channel the situation is even more dramatic because the interferer has a higher power compared to the wanted signal. Therefore either the selectivity of the analog filter has to improve by increasing the order of the AA-filter or the ADC has to have enough dynamic range and linearity to convert in the digital domain the interferer as well. In this way a digital post-filtering will achieve the required selectivity. Due to the fact that in the newer technologies the cost for such kind of digital techniques in terms of power is foreseen to decrease with the time it looks more promising from a power point of view a weak analog filtering followed by a strong digital post-filtering compared to a pure analog approach.

The values of signal, noise and SNR given in Figure 23 have to be intended after decimation is performed. In Figure 23(b), after decimation a SNR equal to about 20 dB is achieved.

Considering the noise factors, they have been calculated with respect to the source impedance driving the stage. The NF values for each block are depicted in Figure 25. The ADC NF is close to 61 dBs with respect to the output impedance of the AA-filter (10 Ω). It is important to notice that, due to the decimation, the new noise bandwidth at the ADC output is one fourth of the Nyquist bandwidth. Therefore the ADC noise power expressed in V_{rms}^2 is given by the following equation

$$V_{rms,ADC}^2 = 10^{\frac{NF}{10}} \times kTR_s \frac{B_{Nyq}}{4} \tag{20}$$

where NF is the ADC noise factor expressed in dB, k is the Boltzmann constant, T is the temperature expressed in Kelvin degrees, R_s is the source resistance of the driving stage and B_{Nyq} is the Nyquist bandwidth (96 kHz in this case). The noise contribution of the ADC is then about 35.5 μV. Now supposing that the ADC FSR is about 0.4 V, the required ADC SNR in dB can be

derived from the following equation

$$SNR_{ADC} = 20\log_{10}\left(\frac{\Delta V_{IN}}{2\sqrt{2V_{rms,ADC}^2}}\right) \tag{21}$$

where ΔV_{IN} is the ADC FSR and $V_{rms,ADC}^2$ is the ADC noise contribution in rms. From equation (21) the required ADC SNR is 72 dB. This corresponds to an effective number of bits (ENOB) which can be calculated from the following equation

$$ENOB = SNR_{ADC} - 1.76 - 10\log_{10}\left(\frac{f_{sample}}{2B_{noise}}\right) \tag{22}$$

where f_{sample} is the ADC sampling frequency. For the system under analysis, this corresponds to 10.67 effective number of bits.

From equations (21) and (22) it can be seen that the SNR due to quantization can be improved by over-sampling the incoming signal. Taking over-sampling to the extreme, it is possible to achieve any desired SNR with one bit sampling at a sufficient high rate. Unfortunately, over-sampling places a bigger burden on the DSP because it increases the bit rate. It can be easily proven that if the SNR is kept constant, and bits of resolution are traded for a higher sampling rate, the overall bit rate increases. This can pose a severe overhead in the DSP stage especially if the overall channel filtering requirements are mainly shifted to the digital domain while leaving a simple low-power AA filter in the analog domain.

It is also important to notice that there is a trade-off between the requirements on the ADC SNR and the maximum gain achievable in the receiver chain without using an AGC. Indeed, the receiver gain strongly depends on the maximum signal the system needs to handle. When the transmitter is at its minimum distance from the receiver, the signal at the ADC input does not have to exceed the FSR. The maximum achievable receiver gain is given by

$$G_{rec}^2 = \frac{FSR^2}{2V_{mix-in,rms}^2} \tag{22}$$

where the factor 2 converts the FSR from peak value to rms value, and $V_{mix\text{-}in,rms}$ is the rms voltage at the mixer input which is equal to

$$V_{mix-in,rms} = V_{in,\max} - L_{BPF} - L_{TX-RX} - L_{Bal} \tag{23}$$

where $V_{in,max}$ is the maximum signal at the receiver antenna and $L_{BPF,}$ $L_{TX\text{-}RX}$ L_{Bal} are the attenuations due to the BPF filter, the TX-RX switch and the balun. Given the values in Figure 22, the maximum voltage gain is limited to 34 dB. The gain along the receiver chain is shown in Figure 26.

The gain achieved till the ADC input is very close to the maximum value of 34 dB. A greater gain will either require a larger ADC FSR (with an increase in the required ENOB) or the use of an Automatic-Gain-Control (AGC) system which will increase the gain when the signal is weak and reduce it when the signal is strong at the cost of decreased sensitivity in the latter case.

A good FOM to characterize the ADC performances is given by the following expression

$$FOM = \frac{P}{2^{ENOB} \times f_{sample}} \tag{24}$$

where P is the power consumption and f_{sample} is the sampling frequency. Supposing a target power consumption of 250 μW, 10.67 effective bits and 192 ksample/s we obtain a FOM equal to about 0.8 pJ/conversion, which is still feasible. It can be noticed that, given the previous FOM, and the equation (22), it is wise to keep the sampling rate low while increasing the ENOB to save power also at the ADC level. Beside this a saving in the DSP power consumption will be achieved given the lower generated bit rate.

Given the previous specifications for the ADC and supposing no AGC system is used, a minimum distance of 40 cm between TX and RX nodes can be achieved without saturating the

ADC.

8.3.Simulation results

The previous theoretical results have been verified by using ADS. A linear model has been built based on a two ports network. The comparison between simulated results and predicted results is shown in Figure 27 and Figure 28. In Figure 28, there is a difference between the predicted SNR and the simulated one. Actually this is due to the fact that in ADS no decimation has been performed and the SNR goes down due to the ADC noise. This is predicted theoretically also, and indeed the gain due to the decimation process is less than the theoretical 6 dB and roughly equal to 4 dB. If no decimation is used the predicted SNR becomes 15.5 dB which correspond to the simulated value.

8.4.Inter-modulation distortion characterization

In a real environment, there is a finite probability that in-band interferers can produce, due to the receiver non-linearities, inter-modulation products which can fall in the band of interest. If the interferers are very strong than it is possible that the resulting inter-modulation product overwhelms the wanted signal.

Interferers can come from other nodes communicating on different channels or other wireless sources using the same bandwidth. The 2.4 GHz band is used also from standards like Bluetooth, Zigbee and WiFi which can act as sources of interferers for the network. In the following analysis only interferers coming from nodes of the same network will be considered. Indeed if coexistence between different standards has to be taken into account, then the selectivity of the ultra-low power node will increase considerably. This increment in the receiver selectivity is not consistent with the ultra-low power target above a certain limit and therefore, an ultra-low power network will be supposed to work properly mainly in a scenario in which other standards or

wireless networks do not constitute the main sources of interference.

For the inter-modulation distortion the first passive blocks in the chain will not be considered. Therefore the three blocks to be considered are the LNA-Mixer block, the AA filter block and the ADC. For the third order inter-modulation distortion calculation, the two interferers to be considered are placed in the adjacent and in the alternate channels. When they mix due to the non linearities in the receiver chain, they generate a third order inter-modulation product (IM_3) which falls in the wanted channel causing degradation in the SNR. The power levels of these two interferers along the receiver chain are depicted in Figure 29. Each of the aforementioned blocks can be described by its input third order input intercept point (IIP_3). Then given the IIP_3, the third order inter-modulation product at the output of each block can be derived using the following equation

$$IIP_3 = \frac{P_{out} - P_{IM3}}{2} + P_{IN} \tag{25}$$

where P_{out} is the alternate channel interferer output power, P_{IM3} is the power of the third order inter-modulation product and P_{IN} is the adjacent channel interferer input power.

From Table I it is possible to highlight possible field of research. Concerning the mixer, given the required gain, NF and IP_3, the use of a merged mixer LNA-mixer topologies requires improvements either in the linearity or in reducing the power consumption. The work in [36] fulfills the gain and NF requirements but it has very poor linearity with a 1dB compression point of only -31 dBm. This figure translates in an IP_3 of about -21.3 dBm, which is very far from the required specification.

The work in [37] meets NF and IIP_3 but it has a current consumption of 8 mA and a conversion gain of 23 dB. Given a 3.4 dB NF there is a good margin to relax the NF and to increase the gain while reducing the power consumption. The AA-filter, as expected, has the largest IIP_3

requirement. Several configurations are feasible for baseband filters:

- g_m-C
- Switched capacitor
- Active RC

Active filter based on OPAMP are more linear than the one using open loop active transconductors. The linearity will be constrained by the linearity of the passive components in the opamp external feedback loop. A switched capacitor topology is also not suitable. Indeed, the filter must be able to handle signal at frequencies well above the channel frequency. Therefore, either the sampling rate becomes unacceptable or the order of the AA-filter has to increase. Both choices lead to an increase in the filter power consumption.

Concluding the best solution in terms of linearity and power consumption is the active-RC filter in which the OPAMP can be designed with transistors biased in weak inversion to reduce the power consumption. In a zero-IF architecture, special care has to be taken to avoid that flicker noise degrades the filter performances. Finally a calibration is needed to correct for the spread in the position of poles and zeros of the filter due to process spread in resistances and capacitances. Nevertheless, this architecture assures very good linearity at reasonable cost in terms of power consumption.

Though the IIP_3 looks quite high it can be achieved with less than 375 μA per pole of the filter transfer function [38]. Indeed, in this work specifications are more tight than required. IIP_3 is higher than required, gain is 18 dB while only 6 dB are required in this work, and worst case input referred noise is 142 $nV_{rms}/\sqrt{Hz}$ for a 100 kHz bandwidth. The noise value is inline with the required specification of 106 $nV_{rms}/\sqrt{Hz}$. To avoid severe constraints on the linearity of the receiver, the SNR degradation due to the third order inter-modulation product has been fixed to

less than 3 dB. This means that to keep the same SNR (20 dB) the signal cannot be at its minimum but 3 dB above. Generally in low power standards like Bluetooth the signal is allowed to be 6 dB above the sensitivity level when inter-modulation is considered. This gives a way to relax further the linearity requirement of the receiver chain. The SNR and the Signal-to-Noise-and-Distortion (SNDR) are depicted in Figure 30. As can be seen from this figure, the presence of the third order inter-modulation product decreases the SNR after decimation by 2.5 dB. If the signal is allowed to be 6 dB above the sensitivity level, like in the Bluetooth standard, then the IP_3 requirements for the LNA-mixer block and the AA-filter can be relaxed to -7 dBm and 17 dBm respectively.

9. Conclusions

The implementation of a micro-Watt network, envisioned in the AmI concept, has a unique set of design constraints that focuses attention on small required bandwidth, low duty cycle operation, short communication range, and the most challenging requirements in average and peak power demand. Nevertheless, a robust wireless link is mandatory, requiring spread spectrum techniques implemented in a low-cost technology.

Reducing the transmission rate reduces the noise floor giving the possibility to increase the noise added by the receiver. This translates in a smaller current consumption for the receiver part. Furthermore, decreasing the data-rate for a given duty cycle allows for a longer synchronization time which is an important parameter in SS radios.

Between the two most common SS techniques (DSSS and FHSS), an FHSS system has been found as the most robust and simple architecture to be implemented in a “micro-Watt node”. The possibility to use the FSK modulation and a switching type PA, together with smaller wake-up time and no need for an AGC system, offers an unique possibility to lower the overall power

consumption by an order of magnitude.

Problems arise due to the complexity of the hopping synthesizer in terms of accuracy and settling time in the frequency synthesis. A new architecture, based on the direct synthesis of frequency bins, is proposed in this article. The proposed architecture reduces the complexity of the hopping synthesizer, reducing by a factor 8 the power consumption with respect to state-of-the-art hopping synthesizers. The required accuracy in the synthesis of the frequency bins is obtained by a combination of digital pre-distortion and offset robust demodulation techniques. In this way, an absolute-accurate synthesizer is obtained and no feedback loop is used [39].

To demonstrate the feasibility of the digital pre-distortion concept, an FHSS transmitter has been realized in SOA technology. Two front-ends have been realized, one based on the common combination of VCO and divider [40] and a second one that reduces the RF front-end to a single block by combining the VCO and the PA.

Measurement results showed the possibility to achieve a BER smaller than 1.1 % at -25 dBm transmitted power, NLOS condition in a common office environment with a distance between TX and RX antennas of around 8 meters. An overall power consumption for the complete FHSS transmitter as low as 2.4 mW at -18 dBm transmitted power has been reported. This is 5 times less than the state-of-the-art FHSS transmitters (see Table II[9]).

Capability to detect small signals in the presence of other interfering signals in a power constrained situation is the main target in the design of an ultra-low power receiver.

A zero-IF architecture is the most suitable architecture for full integration and avoids the IF section which requires additional power. Due to the small signal bandwidth the receiver NF is

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[9] In the table for the transceiver products only the power dissipation in TX mode has been considered for comparison.

relaxed allowing reducing the power consumption both in the LNA and in the mixer.

Considering interferences coming from other nodes of the same network, the IIP_3 requirements are also relaxed. Indeed, the zero-IF architecture concentrates the higher linearity requirements on the AA-filter. In this block noise is of no concern due to the high gain of the LNA-mixer block and therefore linearity is the only target. In the LNA-mixer, instead, the main target is the noise, though an 11 dB NF allows using a small current even at high voltage gain.

Concluding if a low data-rate is employed, NF can be extremely relaxed while linearity will not have severe degradation effect due to the low probability of collision. These architectural choices translates in an overall power optimization without spoiling the transceiver performances.