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RF Building Blocks and Entertainment SoCs for Mobile Telecommunication Platforms

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Abstract

Both for System-in-a-Package (SiP) and Systems-on-a-Chip (SoCs) solutions for applications on mobile telecommunication platforms, power dissipation, size and cost are of prime importance. Advanced CMOS processes allow the introduction of intelligence on chip creating so-called smart SoCs. The vision for these "Smart" SoCs is to re-use programmable resources on-chip for calibration purposes to enhance performance or reduce power consumption. After calibration these resources, e.g. FPGAs, can be re-used for normal system operation. In cheaper main-stream BiCMOS processes complete integration and smartness can be achieved by taking revolutionary choices on the architectural level. Two examples of novel RF architectures are highlighted, which resulted in the first "no-external components" FM radio and TV tuner for mobile telecommunication platforms. Both SoCs make use of resources that are generally available on mobile platforms like a reference clock and a microprocessor to make them "smart". Key RF building blocks of the Entertainment SoCs are discussed in detail. In particular, a wideband LNA, high precision filters and an octave tunable quadrature oscillator.

1. Introduction

Mobile phones are these days packed with features, such that the name mobile phone only refers to one of many possible functions of the portable device. Radio, MP3 player functionality, games, PDA functionality (smart phones) are already a commodity, and soon analog and especially digital TV (e.g. DVB-H) will be accepted as standard features on a mobile phone [1, 2, 3, 4].

All these "add-ons" on top of the primary function of being able to make phone calls and receive them, have similar constraints. Obviously they should be cheap (minimum bill of material and IC die size), the volume a function needs should be minimum, and the power consumption should be a low as possible as the application should not drain the battery of the phone too fast, making it's primary function questionable.

Whether it concerns the above mentioned "Entertainment add-on's" or the actual transceiver for making phone calls with a mobile telecommunication terminal, the choice of technology is crucial for meeting cost, form factor, dissipation, and especially time-to-market requirements. Currently, many transceiver front-ends in telecommunication terminals are in BiCMOS [5], but wireless multi-standard full CMOS SOCs [6, 7] are already a commodity, and also cellular solutions are being developed for 3G terminals in full CMOS [8]. In addition to the implementation technology, a choice has to made between a full system-on-a-chip (SoC) solution or a system-in-a-package (SiP) solution. Apart from all the usual pro and con arguments (see for example [9]) regarding SoC versus SiP, it is difficult to argue against the fact that SoC makes only sense for high-volume products [10]. The nonrecurring engineering (NRE) cost for a state-of-the-art SoC can easily reach $ 10 million if all design engineering, verification, photo masks, and tool cost are taken into consideration. Clearly, many millions need to be sold for such a SoC to bring the NRE cost per device to an acceptable level [10].

Two trends drive innovation and breath fresh air into the SoC approach. The first trend is the addition of flexibility to SoCs by utilizing architectures based on software radio and RF platform approaches [11]. This addresses also the need for multi-standard front-ends that is required for 3G and 4G telecommunication platforms, as the increased flexibility can allow re-use of hardware for multiple standards. The second trend is making SoCs increasingly smart by adding intelligence to each (RF) building block on the IC. This intelligence can offer detection and control, adaptivity,

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correction, self-testing, redundancy, etcetera, that in turn increases the yield and functionality of the building blocks on the SoC as well as that of the total system. The increased flexibility that RF platforms can bring is discussed in [12].

This paper discusses first the smart approach in more detail in Section 2. In Section 3, two complete receivers, an FM Radio and TV entertainment SoC for mobile platforms are highlighted. Next, in Section 4, some of their digitally controlled, smart, RF building blocks (LNA, oscillators, filters,...) are discussed. Both BiCMOS ICs show that by making use of resources (microprocessor, clock, and user interface) available on the mobile platforms, and by adding intelligence to each RF building block, all external components can be eliminated for portable Radio and TV receivers.

2. Smart SoCs

On-going scaling in IC technologies and the higher integration densities increasingly complicate analog design. On top of that, testing and yield are becoming a major bottleneck, both for general-purpose chips and dedicated system-on-chip designs [13]. CMOS scaling means for the analog circuitry (e.g. receiver front-ends) that the accuracy goes down, spread gets worse, and so is yield and reliability [14]. On top of that systems are getting complexer (e.g. compare GSM versus 3G) and design cycles are under constant pressure to shorten because of time-to-market requirements.

One approach to deal with these challenges is to increase the programmability of the SoCs and add intelligence and robustness in ever sub-system of the SoC. This is increasingly made easy as many full-custom ASICs have evolved towards full-custom SoCs, with programmable cores, like DSPs, and recently even with FPGA cores [13]. Especially in case of FPGA or DSP cores available on the SoC, the hardware and resources required to make the IC "smart" in order to:

- increase the integration density;
- widen the application range;
- widen the achievable performance range;
- increase yield, reliability and robustness;
- alleviate test problems and lower test costs.
- ...

can be kept low. No substantial extra hardware resources might be required for the quite complex digital signal processing, when large amounts of digital programmable resources are already available on-chip that can be used during free time slots in an application.

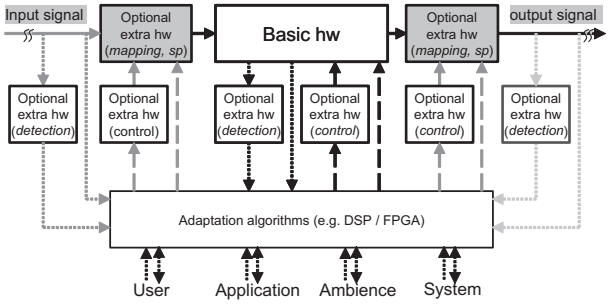

Figure 1. Conceptual block diagram of smart building blocks.

In Fig. 1 a generic diagram of the smart building block, pointing out all possible options, is visualized. The various information streams, that can be used for circuit optimization, are drawn (dotted lines); the information can be obtained from the signals (input/output or intermediate signals), the system (the basic hardware, including the error sources, or additional hardware to detect process status parameters or e.g. temperature), or the environment (users, application, ambient conditions). Reference information is principally required to do judgements on performance.

The optional dedicated hardware components in Fig. 1 are for detection (of signal spread parameters, temperature, process spread, etc.), for control (calibration, swapping, biasing, etc.), and for extra mapping or signal-processing. The mapping or signal-processing hardware is included in the signal path. It facilitates adaptable static and dynamic signal manipulations, e.g. for de-correlation or dynamic element and adaptable filtering, pre-correction, post-correction, etc. That CMOS SoC's become increasingly smart is evident from implementations highlighted in [6, 7, 8], for example.

In BiCMOS, integration of large amounts digital cores or dedicated is less self evident as the chip area of these digital circuits will be always significantly larger (more expensive) compared to state-of-the-art CMOS processes that have a smaller feature size. However, as will become clear in the reminder of this paper, by making use of available processing power on portable platforms, "smart" BiCMOS entertainment SoCs can be realized without any external component.

3. Smart BICMOS entertainment SoCs

On mobile platforms such as phones, a micro-processor, a reference oscillator, and user interfaces are readily avail-

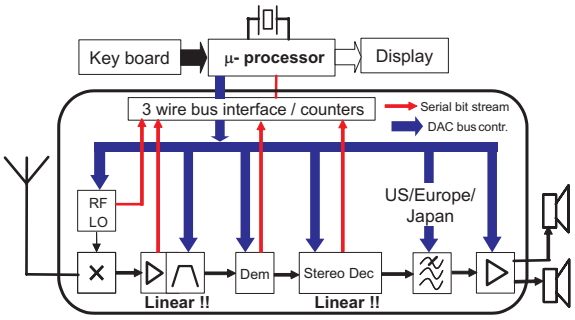

Figure 2. Block diagram of the no-external components FM radio.

able. These resources are also used in the case of the FM radio architecture shown in Fig. 2 [15]. A low-IF architecture is chosen like in [16]. After down-conversion of the desired channel, fully integrated selectivity has been implemented. The improved selectivity filters are temperature compensated and digitally programmable. In this way the micro-controller can correct not only the spread in the process parameters, but also can perform circumstantial control functions like reduction of the bandwidth [16] in poor reception conditions. The adjustment of all characteristic frequencies of filters and oscillators will be performed by the micro controller. Due to the use of frequency locked loops (FLLs) instead of phase locked loops (PLL) the frequency of the crystal can be freely chosen to achieve minimum overall cost. For the control of the RF oscillator a capacitance bank is used to improve the ripple rejection and to avoid a large and noise sensitive tuning voltage [17].

Technology:	BICMOS 9 GHz f_T/ 0.6 µm
Chip area (mm²):	11
Power (mW):	46 (at 2.7 V)
Supply voltage (V):	2.7 - 7
Sensitivity (µV):	1
Image rejection (dB):	26
Stereo chan. sep. (dB):	30
THD (%):	0.7

Figure 3. FM radio specifications summary.

The whole radio signal path is controlled by several AGC's to process all signals in a linear mode. This is to avoid intermodulation products, folding and repeat spot reception. The result is shown in the improved dynamic selectivity. The IF frequency is chosen at 110 kHz to allow 30% overmodulation. Due to this choice the image reception is positioned in the slope of the dynamic selectivity. The key elements that enabled zero external components for this "smart

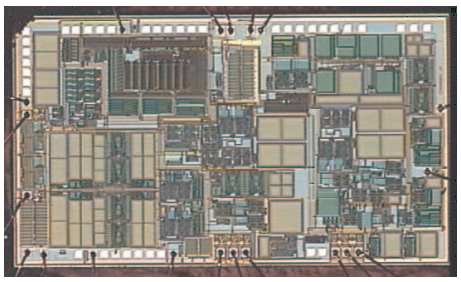

Figure 4. FM radio receiver die photo.

Entertainment FM-radio SoC" are a high performance analog signal processing path with many dedicated novel IP blocks that are all software controlled, and re-use, where possible, of the platform resources.A performance summary of the radio IC is given in Fig. 3.

The FM radio IC is implemented in a 8 GHz f_T mainstream BiCMOS technology. Fig. 4 shows the chip micrograph. The total active chip area is 11 mm2. Its total power dissipation is 17 mA with a nominal supply voltage between 2.7 and 7 Volt.

Fig. 5 highlights the architecture of the Universal Mobile TV (UMTV) chip [18]. No front-end antenna filter is required because the LNA has built-in tunable selectivity (it's operation is described in the next section). After the LNA a system of mixers suppresses harmonics and a low-IF polyphase filter follows. A feature of this fully integrated filter is that it can suppress the image up to 60 dB (Dynamica Image Suppression: DIS). Channel selectivity is followed by a split filter after which sound and video are demodulated. A low-IF quadrature output is provided for digital DVB-H demodulators. For the sound demodulator, the demodulator of the described FM radio could be fully re-used [15]. Identical to the FM radio, UMTV does not require external components. Also, every RF and IF building block is made smart by adding software control.

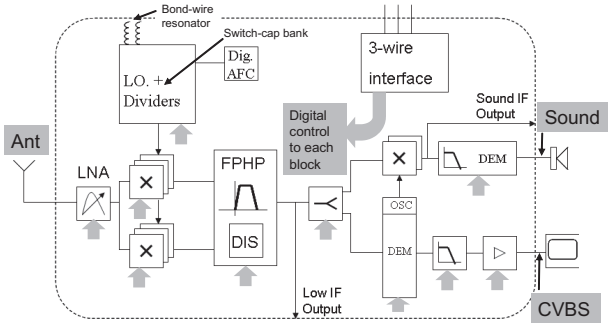

Figure 5. Block diagram of UMTV.

The UMTV IC is realized in a low-cost mainstream 8 GHz f_T BiCMOS process and dissipates 150mW. The die photo (size 5*5 mm) of the complete multi-standard TV receiver is shown in Fig. 6. Total noise figure of the TV receiver is less than 9 dB and its 1 dB compression point is more than 80 dBμV.

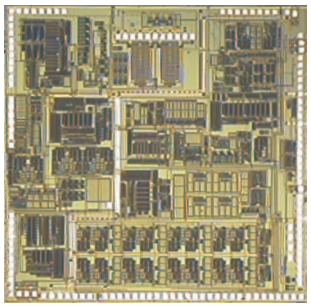

Figure 6. UMTV die photo.

4. High performance RF building blocks

The discussed architectures of the radio and TV receiver both rely heavily on high performance signal processing blocks that are microprocessor controlled and allow through calibration and adaptivity, high quality signal processing. Three RF blocks that are used in these architectures are described in this section.

4.1 Low noise tunable amplifier

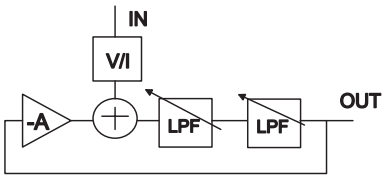

Figure 7. Broadband tunable amplifier.

The signal processing of the UMTV chip starts with a selective tunable Low Noise Amplifier (LNA). It plays a crucial role in obtaining the targets for a high sensitivity and a low power dissipation. The principle of the selective LNA is illustrated in the block-diagram in Fig. 7. The antenna signal is converted from voltage to current (V/I block). This current is injected in the loop of an inverter amplifier with gain -A and two low-pass filters (LPF). The cutoff frequency of the LPFs can be controlled with currents. The positive feedback with a phase shift of approximately 360° in the loop (180° due to the inverter and approximately 180° by the low pass filters) will tuned to different frequencies. By controlling the total gain in the loop, sufficient phase margin at gain > 1 is obtained to keep the loop stable. By making more phase shift in the loop (e.g. by adding more orders to the LPF), the quality factor will be higher and the shape of the curve will change. For an LNA to keep the noise at a low level, it is important to keep component count of the signal processing components as low as possible. This wideband tunable LNA concept can be designed in silicon with only 5 transistors and no dominant resistors in the signal path [18]. The selectivity curves of the LNA are given in Fig. 8. Frequency responses for various tuning currents are shown. The noise figure of the LNA plus mixers and IF filter (see Fig. 5) is always better than 9 dB over the total VHF and UHF band (40 MHz to 900 MHz) [18].

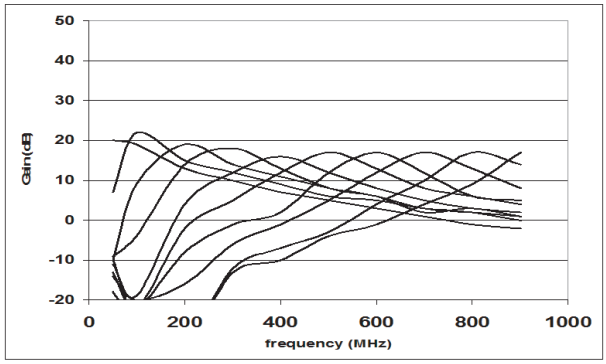

Figure 8. Measured selectivity curves.

4.2 Programmable high precision filters

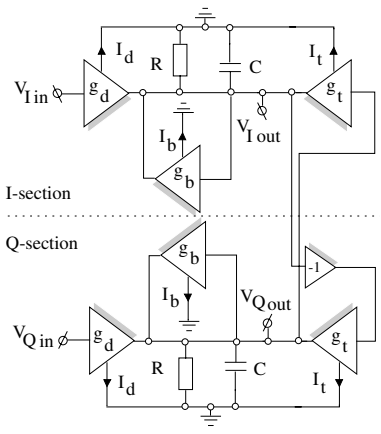

Figure 9. Behavioural model of one filter stage.

The FM receiver as well as the UMTV SoC make use of microprocessor controllable high-precision filters The behavioral diagram of one filter section is shown in Fig. 9. In this figure the three transconductances, g_t, g_b and g_d control the bandpass center frequency, bandwidth and gain. The center frequency is equal to $g_t/(2\,\pi\,C)$. Transconductance g_b in the I and Q sections implements a negative resistance of $-1/g_b$ which is in parallel with R. The resulting resistance R_{tot} is used to control the bandwidth of $1/(\pi\,R_{tot}\,C)$. The gain at the center frequency is $g_d\,R_{tot}$.

4.3 Digitally programmable octave tunable oscillator

A crucial subfunction of the UMTV chip is the local oscillator. It is a quadrature oscillator circuit with integrated digital capacitance bank [15, 18] with a tuning range from 420 to 900 MHz. One section of the oscillator is shown in Fig. 10. The resonator in each section makes use of bondwire inductors, which are together with the capacitor bank connected to i_{tank}. Unlike most I/Q oscillators no cross-coupled pair (thus eliminating a self-oscillation mode) is present within a section, making the circuit very robust against multi-mode oscillations, which are well-known in I/Q oscillators. Transistors Q7 and Q8 together with their external (and internal) base resistors implement active inductors that tune the total phase shift of each section close to 90°, thus realizing operation at the resonance frequency of the LC-tank circuit where the quality factor is maximum.

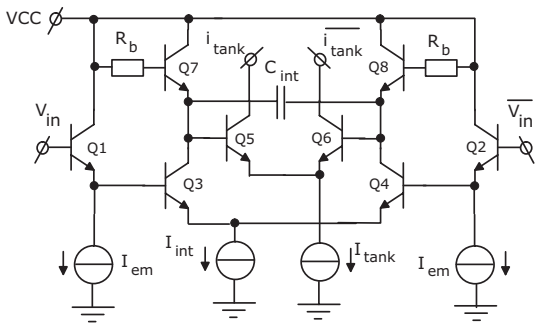

Figure 10. Octave tunable I/Q oscillator.

5. Conclusions

A generic view on "Smart" SoCs has been presented in this paper. Gradually smartness has entered RF front-ends. Descending from system level to sub-systems, digital control and adaptivity will eventually perhaps even reach the transistor level. Two "Smart" innovative entertainment SoCs with no-external components are highlighted in this paper. The FM radio achieves a sensitivity of 1 μV and occupies only 11 mm^2. The multi-standard TV receiver dissipates only 150 mW, covers all analog standards, and has a low-IF output for digital standards. Both ICs demonstrate how HW/SW co-design and smartness in low-cost BiCMOS processes, can eliminate all components, minimize required board space, while maintaining a high performance level for complex applications like complete FM radios and TV receivers on mobile telecommunication platforms.

Acknowledgment

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