

# Minimum Power-Consumption Estimation in ROM-Based DDFS for Frequency-Hopping Ultralow-Power Transmitters

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**Abstract**—The future of all kinds of applications that require a submilliwatt consumption strictly depends on the capability to meet design specifications at the minimum power costs. While several computer-aided-design tools are present to estimate the power consumption of modern ICs at transistor level, it is very difficult to predict the power at higher level. Given the reduced time-to-market of modern communication devices, it is very often needed to have accurate power estimations prior to the transistor-level design. Allocating a too conservative power budget to a block implies a possible poor tradeoff between the specifications of building blocks that constitute the system and their power consumption. For future power-constrained wireless devices (like wireless nodes in sensor networks), it is very important to have high-level models which can help the designer with the initial high-level choices without going into transistor-level design. One of the important blocks in modern communication devices, particularly for spread-spectrum systems, is the frequency synthesizer. In this paper, the first power-consumption model for an ultralow-power ROM-based direct digital frequency synthesizer has been developed, which can help the designer in the power optimization at a high level prior to transistor implementation.

**Index Terms**—Direct digital synthesizer (DDS), frequency hopping (FH), low power, power estimation, sensor networks.

## I. INTRODUCTION

**M**ANY WIRELESS applications in the consumer home today, and in the ambient intelligent home of the future, require only very low data rates ( $< 10$  kb/s) and can accept a low quality of service.

At the same time, the overall power consumption must be minimized in order to have an autonomous wireless node, which can harvest the required energy from the environment. Moreover, a robust link is required in the harsh indoor environment.

Commonly referred to as frequency-hopping spread spectrum (FHSS), hopping across multiple frequencies is a proven

way to sidestep interferences and overcome RF challenges by using agility rather than brute force (i.e., increasing the transmitted power). Another technique to increase the robustness of the radio link is the direct-sequence SS. Nevertheless, this technique is not sufficient in the face of common interferers (like Wi-Fi or Bluetooth) without a significant increase in the processing gain. This can make the power consumption higher due to a longer synchronization time and increased operating frequency of the baseband circuitry [1].

The most critical block in an FH wireless system is the synthesizer. The two most common ways to implement an FH synthesizer are the phase-locked-loop (PLL)-based synthesizer and the direct digital synthesizer (DDS). The major drawback in a PLL synthesizer is that it is a closed-loop system, and power and settling time are tied together [2]. This means that the PLL requires a certain time to change the output frequency. This time is quite long due to the fact that a pull-in process can be required in the most general case.

When some channels experiment deep-fading conditions, the capability to increase the hopping rate gives a way to avoid an increase in the transmitted power while still correctly demodulating the signal. This capability should not cause any increment in the overall power consumption particularly at high hopping rate. In this sense, a PLL-based synthesizer does not fulfill the requirement. On the other hand, a DDS has a settling time which is small and independent from the power consumption because no feedback loop is involved in this architecture.

In a power-constrained environment, it is important to optimize the system in such a way that the specifications are the minimum required (with some extra margin) to have a robust wireless link. In this way, the system can be designed for the minimum power consumption rather than for the best performance. Starting from this assumption, the prediction of the power consumption in a DDS system becomes critical in order to set the specifications of each subblock in the DDS in such a way to minimize the overall power consumption.

Several architectures have been developed for the direct digital frequency synthesis. They can be divided into two large groups: ROM based and ROM-less.

The ROM-based direct digital frequency synthesizers (DDFSs) use a ROM to convert the phase information into an amplitude information. This ROM can be sometimes very large and, therefore, very power hungry. For this reason, several improvements to this architecture have been developed in order

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to reduce the ROM size. Some of these modified architectures are the following [3]:

- 1) modified Sunderland architecture;
- 2) modified Nicholas architecture;
- 3) Taylor series expansion;
- 4) cordic algorithm;
- 5) quarter wave symmetry.

All of these improved architectures can compress the ROM considerably, saving therefore a large amount of power particularly when the ROM is large. However, as it will be proven in Section IV-B, in DDFSs designed for ultralow-power transmitters, the ROM contributes only less than 15% to the overall power consumption. For this reason, these improved architectures will not be crucial here and, thus, will not be considered further in this paper.

ROM-less architectures manage to remove completely the ROM. The phase-to-amplitude conversion is performed using interpolation algorithms or nonlinear digital-to-analog converters (DACs) [3]. These ROM-less architectures achieve good performances when the synthesized frequency is very low as compared to the clock frequency. In the proposed case, the maximum synthesized frequency is around 15 MHz. The clock frequency must be kept low in order to have a low-power clock generation. As it will be clear in Section V, the clock frequency is around 100 MHz and, therefore, comparable with the maximum synthesized frequency. Furthermore, considering that the ROM is not the dominant contributor to the overall power consumption (see Section IV-B), these ROM-less architectures will not be discussed further in this paper, and a simple ROM-based DDFS is considered throughout the following sections.

This paper is organized as follows. In Section II, the DDS high-level specifications are derived, and in Section III, they are translated in per-block specifications. In Section IV, the DDS power-consumption model is disclosed, while results are given in Section V. Section VI concludes the paper.

## II. DDS SPECIFICATIONS FOR ULTRALOW-POWER FH TRANSMITTERS

A typical FH transmitter architecture employing a DDS as baseband synthesizer is shown in Fig. 1. Modulation can be simply added in the digital domain when a simple binary frequency-shift keying (BFSK) modulation is used. Therefore, it has been omitted in Fig. 1. The TX architecture utilizes a direct up-conversion. This choice reduces the number of high-frequency stages, reducing, in this way, the overall power consumption. On the other hand, it requires a quadrature baseband signal and, therefore, two DACs and two antialiasing (AA) filters. To reduce the power consumption at baseband, the direct up-conversion is performed in a single-sideband (SSB) fashion. This choice halves the maximum output frequency of the DDS [4].

FCC rules demands for at least 25 hopping channels (20-dB channel bandwidth greater than 250 kHz) in the 902–928-MHz band and 15 channels in the 2.4-GHz ISM band. This paper will address the generation of 50 hopping channels, which will

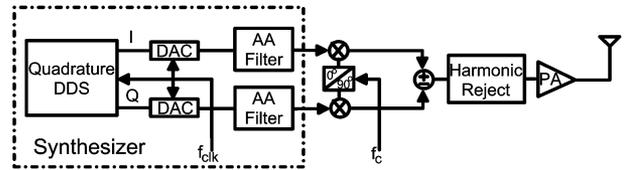


Fig. 1. Simplified block diagram of an FHSS transmitter employing a DDS.

cover also the restriction on the 902–928-MHz band, which requires 50 hopping channels if the 20-dB bandwidth is smaller than 250 kHz. Given the fact that an SSB up-conversion scheme will be used at the transmitter side, it is necessary to synthesize 25 hopping channels in the DDS. If two adjacent hopping channels are separated by 0.6 MHz, then the range of frequencies varies between 0.6 and 15 MHz with a 0.6-MHz frequency step. Furthermore, from now on, a wideband FSK modulation is considered as a modulation format.

The choice of such a large spacing between the adjacent channels even for a data rate, which is supposed to be below 10 kb/s, is dictated by the necessity to have a certain frequency diversity in the indoor environment. Using the statistical approach, the coherence bandwidth is defined as the bandwidth over which the fading statistics are correlated to better than 90%. Clearly, if two frequencies do not fall within the coherence bandwidth, they will fade independently. The delay spread in a channel can be used as a figure of merit to calculate the coherence bandwidth. In typical indoor environments, the delay spread is around 50 ns at 2.4 GHz [5]. The coherence bandwidth for a 90% correlation is given by the following relation:

$$BW_c \simeq \frac{1}{50\sigma_\tau} \quad (1)$$

where  $BW_c$  is the coherence bandwidth and  $\sigma_\tau$  is the delay spread. Therefore, in the 2.4-GHz environment, the coherence bandwidth is around 400 kHz. Hence, the choice of a 0.6-MHz channel spacing makes the channel to fade more independently.

As aforementioned, the range of applications is limited to low-data-rate applications with an average data rate of up to 10 kb/s. The modulation used is BFSK with a modulation index larger than one to reduce the effect of nonidealities at the receiver side during demodulation.

As any sampled system, a DDS will have an image frequency which needs to be attenuated by the AA filter. Besides the image frequencies, a number of spurs and harmonics will appear in the spectrum due to the digital truncation used in the synthesis process. During transmission of a certain frequency, it is necessary to keep the unwanted spurs below a certain level. They will generally pollute other channels, causing cochannel interference to other nodes communicating on those channels.

In [6], it is shown that 30-dB rejection of the image signal is largely sufficient to avoid the deterioration of the bit error rate of the transmission. Considering an extra margin of about 10 dB to take partially into account the fading condition on the wanted signal, a 40-dB required rejection has been considered. Moreover, given the fact that, for the up-conversion, a SSB scheme is used, due to process spread, the image will not be rejected perfectly. A common figure of merit for harmonic rejection is about 40 dB and, in general, higher degrees of rejection

TABLE I  
DDS REQUIREMENTS

	Spec.	Unit
Maximum frequency	15	MHz
Minimum frequency	0.6	MHz
Resolution	6	Hz
SFDR	46	dB

require complex calibration techniques. Given an extra implementation margin of 6 dB, the overall required spurious-free dynamic range (SFDR) for the synthesizer can be set at 46 dB.

The frequency accuracy of the DDS should not limit the choice of the FSK demodulator topology. The most stringent requirements in terms of frequency offset come from the correlation-based demodulator [7]. For example, for a data rate of 3 kb/s,<sup>1</sup> a 10-ppm accuracy is a suitable choice (worst case offset is 300 Hz). This translates in a 6-Hz resolution when a 0.6-MHz frequency is synthesized.

The reference clock frequency, the required number of bits in the accumulator, the amplitude word length, and the AA filter order are all parameters which will be evaluated and adjusted in order to find the best tradeoff between power consumption and system requirements. Table I summarizes the DDS specifications for the ultralow-power transmitter.

### III. DDS BUILDING BLOCKS SPECIFICATION

As shown in Fig. 1, the digital and the mixed-signal parts are clocked by the same reference frequency ( $f_{\text{clk}}$ ). A DDS is a sampled system. This means that the minimum frequency at which the system has to operate is dictated by the Nyquist theorem, and it needs to be twice the maximum signal frequency. In this specific case, it is 30 MHz. Unfortunately, this is just the theoretical limit, and it will make the filtering of the image frequency impractical. Therefore, the minimum reference clock frequency ( $f_{\text{clk}}$ ) has to fulfill the following rule of thumb:

$$f_{\text{clk}} \geq \frac{f_{\text{max}}}{0.4}. \quad (2)$$

This means that the reference clock frequency has to be larger than 38 MHz for a maximum wanted signal ( $f_{\text{max}}$ ) of 15 MHz. At a glance, it is possible to recognize that increasing the clock frequency will reduce the filter complexity (and therefore, most probably, the filter power consumption) but will increase the power consumption of the digital part and probably of the DAC. It is therefore imaginable that an optimum exists, which minimizes the overall power consumption.

The digital part of a DDS is shown in Fig. 2. This kind of architecture is similar to a numerically controlled oscillator. The output of the phase accumulator is linear, and therefore, it can only generate a ramp but not a sine wave. A phase-to-amplitude lookup table is used to convert a truncated version of the phase accumulator's output into a sine-wave amplitude information, which is then the input of a DAC. The frequency control word (CW) has  $M$  bits and sets the output frequency. Indeed, if we

<sup>1</sup>Smaller data rates are possible but they will require a larger number of bits in the phase accumulator.

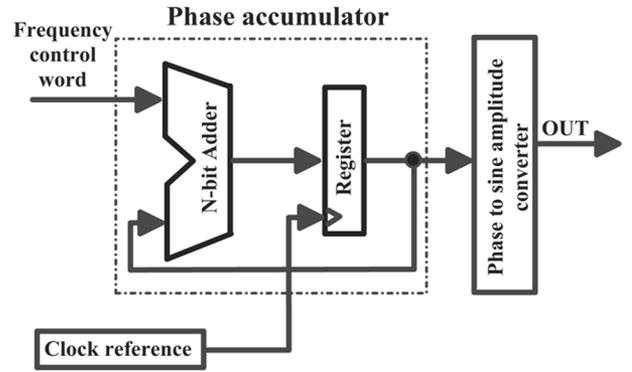


Fig. 2. Simplified block diagram of the digital part of a DDS.

consider an  $N$ -bit phase accumulator, the output frequency will be simply given by the following relation

$$f_{\text{out}} = \frac{\text{CW} \times f_{\text{clk}}}{2^N}. \quad (3)$$

The number of bits in the phase accumulator depends on the frequency accuracy required. The frequency resolution is given by the following relation:

$$f_{\text{res}} = \frac{f_{\text{clk}}}{2^N}. \quad (4)$$

Therefore, the minimum number of bits in the phase accumulator is found by inverting the previous relation and approximating the result to the greater integer. Of course, this requires one to know the reference clock.

The first tradeoff can be easily foreseen. Increasing the clock frequency will require a larger accumulator working at a higher frequency (more power) but it will relax the specification on the AA filter. Anyhow, the minimum number of bits can be derived for the minimum frequency requirements (40 MHz). This yields an accumulator with at least 23 bit. When the final clock frequency will be chosen, this value might be different by 1 or 2 bit. In Section IV-B, it is shown that the accumulator negligibly contributes to the overall power consumption in modern CMOS technology. For this reason, the word length will be kept fixed to 23 bit.

The output of the phase accumulator addresses a ROM in which the amplitudes of a sine wave are stored. In practice, the ROM limits the usable length of an input phase word<sup>2</sup>. Therefore, the phase word length is larger than the ROM address word length, and simply, a truncation is used on the phase word. This is one of the main sources of spurious tones in the output spectrum of a DDS.

The harmonic content at the output of the DDS will be thus determined by three main sources.

- 1) Images of the fundamental frequency due to sampling nature of the system.

<sup>2</sup>A 23-bit word for the phase information is a moderate choice in DDS applications. If every phase step is mapped in an amplitude step with, for example, 8-bit precision, then a 64-Mbit ROM would be required. This can be reduced to 16 Mbit if the quarter-wave symmetry of the sine is exploited but it is still a too large value for a power-constrained system.

- 2) Spurs from the phase truncation and DAC quantization error.<sup>3</sup>
- 3) Harmonics of the fundamental frequency due to DAC integral nonlinearity (INL).

The image filter mainly affects the filter requirements in terms of filter order. A DAC has, at the output, a sample-and-hold functionality. The effect of this block is to shape the frequency components of the wanted signal in a  $(\sin(x))/(x)$  fashion, where  $x = (\pi(f_{\text{clk}} - f_{\text{max}}))/(f_{\text{clk}})$ . Given the fact that the system will synthesize one frequency at a time, this does not constitute a problem. This characteristic can also be used to relax the filter specifications, introducing some oversampling. Therefore, in the worst case condition of a 40-MHz reference clock, the first image frequency will be attenuated by roughly 6.5 dB.<sup>4</sup> The attenuation required by the AA filter in the worst case condition is therefore around 40 dB. Phase truncation plays a big role in setting the SFDR of the DDS. The maximum spur at the output of a DDFS system in case of a truncation larger than 4 bit is upper bounded by  $-6.02P$  dBc [8], where  $P$  is the number of bits in the truncated phase words. To not spoil the SFDR of the system, a 46-dB figure is required. This translates in at least an 8-bit phase-word address for the ROM (phase-to-amplitude converter). Therefore, with an 8-bit phase word, an SFDR of around 48 dB is achieved.

The number of bits in a DAC is determined by its required spurious performances. Spurs in the DAC come from both the quantization error (see <sup>3</sup>) and the DAC INL. The level of the highest spur due to phase truncation is 48 dB. To reasonably derive a specification for the DAC, the approach in [9] is used. If the sum of all the harmonics due to phase truncation is considered as “noise,” then a signal-to-noise ratio (SNR) can be defined when only phase truncation is considered. Now, given the large truncation used for the phase word (from 23 to 8 bit), the following expression can be used:

$$\frac{S}{N_{\text{phase}}} = 6.02P - 5.17 \quad (5)$$

where  $S$  is the signal power and  $N_{\text{phase}}$  is the noiselike power due to spurs coming from the phase truncation. Therefore, the SNR of the truncated phase signal is around 43 dB. The DAC should contribute negligibly to the overall noise,<sup>5</sup> and therefore, the required SNR for the DAC has to be larger than 49 dB. From [9], it can be proven that, because the quantization errors are not evenly distributed in one period because of the shortness of the period (e.g., when the maximum frequency is synthesized), the SNR at the DAC output is given by the following relation:

$$\frac{S}{N_{\text{DAC}}} = -3.01 + 6.02N_{\text{DAC}}. \quad (6)$$

This translates in  $N_{\text{DAC}}$  of 9 bit.

<sup>3</sup>The quantization error is generally treated as white noise. In a DDS, this approximation is valid only in the limiting case when the numerical repetition period of the ROM quantization error is long. In our case, the maximum output frequency is comparable with the clock frequency (see Section V), and therefore, this approximation is not valid anymore. In the case of a short numerical period of the ROM quantization error, a number of spurs will appear around the fundamental as an effect of the amplitude quantization in the DAC.

<sup>4</sup>The first image frequency is in the worst case at  $f_{\text{clk}} - f_{\text{max}}$ , where  $f_{\text{max}}$  is the maximum signal frequency.

<sup>5</sup>It is important to highlight that this noise does not show a flat continuous spectrum but that it is made up by a large number of spurs due to the phase truncation and quantization error in the DAC.

TABLE II  
NUMBER OF POLES IN THE FILTER PER OCTAVE INCREMENT IN THE DISTANCE BETWEEN WANTED SIGNAL AND IMAGE FREQUENCIES

	Number of poles	Clock frequency [MHz]
One octave	7	45
Two octaves	3	75
Three octaves	2	135

Lastly, from the SFDR specification, the required maximum INL is readily calculated by the following [10]:

$$\text{INL} = \frac{1}{\text{SFDR}} - 2^{-1.5N_{\text{DAC}}} \quad (7)$$

where the INL is expressed in LSB. Given a 46-dB required SFDR, the maximum allowed INL is 2.5 LSB.

#### IV. DDS POWER-CONSUMPTION ESTIMATION

The power consumption of the DDS will be derived considering the power consumption of each block at different clock frequencies. Then, the frequency which minimizes the overall power consumption will be chosen as the optimal solution. Given the fact that the choice of the reference clock frequency will heavily affect the filter design, the choice will depend mainly on the filter specifications. In this sense, the reference clock frequency is chosen in such a way that the first image frequency in the worst case condition is placed one, two, or three octaves far from the maximum wanted signal. For  $f_{\text{clk}} \geq 10k \times f_{\text{max}}$ , the filter can be implemented completely in a passive way and have virtually zero power consumption. Following this procedure, the following analysis will be carried out at  $f_{\text{clk}} = k \times f_{\text{max}}$ , where  $k = 3, 5,$  and  $9$ .<sup>6</sup>

##### A. AA-Filter Power Consumption

The first step consists in evaluating the required filter order for a given required attenuation. Supposing a 6-dB extra margin on the minimum required attenuation of 40 dB, the filter must attenuate the image frequency by around 46 dB. Each pole attenuates the unwanted image frequency by 6 dB/octave. Furthermore, the amplifier at the DAC output will have a bandwidth roughly equal to the maximum signal frequency. Therefore, it will act as a first-order filter for the image frequency. Table II summarizes the required number of poles depending on the position of the first image frequency.

The estimation of power consumption in LPFs can be derived following the work in [11]. We will shortly go to the set of equations useful to derive the filter’s power consumption.

The basic parameters required for a correct estimation are the noise excess factor ( $\xi$ ) and the required dynamic range (DR). The first step is to evaluate the required DR. Now, the noise level at the DAC has been set to 52 dB below the signal level in the bandwidth of interest. The AA filter must negligibly contribute to the overall noise. Therefore, the noise of the filter in the same bandwidth must be at least 6 dB below the noise contribution

<sup>6</sup>The position of the image frequency is supposed to be  $2f_{\text{max}}$  or  $4f_{\text{max}}$  or  $8f_{\text{max}}$ . Now, considering that the image frequency is at  $f_{\text{clk}} - f_{\text{max}}$ , then  $f_{\text{clk}}$  has to be 3, 5, or 9 times the  $f_{\text{max}}$ .

TABLE III  
BUTTERWORTH NORMALIZED POLYNOMIAL COEFFICIENTS, OVERALL FILTER CAPACITANCE, AND PREDICTED POWER CONSUMPTION

Filter Order	c <sub>0</sub>	c <sub>1</sub>	c <sub>2</sub>	c <sub>3</sub>	c <sub>4</sub>	c <sub>5</sub>	c <sub>6</sub>	c <sub>7</sub>	Capacitance [pF]	Power consumption [mW] <sup>a</sup>
2	1	1.414	1	-	-	-	-	-	4.16	0.157
3	1	2	2	1	-	-	-	-	94.5	0.535
7	1	4.494	10.098	14.592	14.592	10.098	4.494	1	386	51

<sup>a</sup>At  $V_{\text{supply}} = 1\text{V}$  and  $V_{\text{max}} = 0.2\text{V}$

coming from the DAC. This means that a 58-dB DR for the AA filter is required.

With these inputs and starting from the state-space representation of the wanted filter, the following equation holds:

$$\text{DR} = V_{\text{max-rms}}^2 \frac{\frac{1}{2\pi} \int_{-\infty}^{\infty} |(j\omega)|^2 d\omega}{\sum_{i=1}^n S_{n,i}(\omega)} w_{ii} \max_j k_{jj}. \quad (8)$$

Now,  $w_{ii}$  and  $k_{jj}$  are the diagonal elements of the matrices  $W$  and  $K$  which can be obtained by solving the following Lyapunov equation sets:

$$A^T W + W A = -C^T C \quad (9)$$

$$A K + K A^T = -B B^T \quad (10)$$

where the upper index  $T$  indicates the transpose matrix and  $A, B, C$ , and  $D$  are matrices in the state-space representation.<sup>7</sup>  $H(j\omega)$  is the normalized filter transfer function.<sup>8</sup>  $V_{\text{max-rms}}$  is the maximum rms voltage the integrators in the filter can handle without introducing a large nonlinearity. If a 1-V supply is considered and a margin of 600 mV is taken, then  $V_{\text{max-rms}} = (0.2)/(\sqrt{2})$ . Finally,  $S_{n,i}(\omega)$  are the input-referred noise spectra of each integrator, and they are equal to

$$S_{n,i}(\omega) = \frac{2kT\xi}{C_i} \left( |b_i| + \sum_{j=1}^n |a_{ij}| \right) \quad (11)$$

where  $k$  is the Boltzmann constant,  $T$  is the temperature in degree Kelvin,  $C_i$  is the capacitance at the output of each integrator,  $b_i$  are the elements of the matrix  $B$ , and  $a_{ij}$  are the elements of the matrix  $A$ .

Supposing all the capacitances equal to a value  $C$ , the only unknown in (11) is  $C$ , which can be derived for various filter orders. In Table III, the coefficients for the Butterworth filters are shown for the three different filter orders derived previously in this section. The required capacitor values in the three cases are also given in the same table. The excess noise factor has been assumed to be equal to 7 [12].

At this point, each integrator must be able to output the wanted signal in the worst case condition and given the capacitance value required to achieve the DR. Considering the signal, a pure sinusoid at the maximum frequency of 15 MHz, we can write the following:

$$I = C \frac{dV}{dt} \quad (12)$$

$$V = V_{\text{max}} \sin(\omega_{\text{max}} t) \quad (13)$$

<sup>7</sup>  $D$  is zero for any practical single-input-single-output time-invariant system.

<sup>8</sup> The normalized filter has a bandwidth equal to one. If the bandwidth is  $\omega_c$ , then the matrices  $A$  and  $B$  should be multiplied by  $\omega_c$ .

TABLE IV  
PHASE-ACCUMULATOR POWER-CONSUMPTION ESTIMATION

Clock frequency [MHz]	Power consumption [ $\mu\text{W}$ ]
45	40
75	60
135	96

where  $V_{\text{max}}$  is the sinusoid peak voltage (0.4 V can be a suitable choice). From (12) and (13), we obtain that, to keep the distortion low, the bias current has to be equal to the peak current delivered to the integrating capacitance and therefore

$$I_{\text{bias}} = 2\pi C f_{\text{max}} V_{\text{max}}. \quad (14)$$

With these values, the predicted current consumption for the three different filters is summarized in Table III.

### B. Phase-Accumulator and ROM Power-Consumption Estimations

The phase-accumulator power estimation can be quite cumbersome due to the fact that the dynamic power consumption mainly depends from the statistics of the signal applied to a certain level of logic ports. For this reason, instead of developing an involved model for the power consumption, the block has been simulated in a CMOS 90-nm process, and the results are given in Table IV. As can be seen, the power consumption is low as compared to the AA-filter power consumption. On the other hand, the power consumption can be easily scaled up or down for different technologies and frequencies by using the following:

$$P_{\text{acc}} = f_{\text{clk}} C_T V_{\text{dd}}^2 \quad (15)$$

where  $V_{\text{dd}}$  is the supply voltage. Therefore, the power scales linearly with frequency and also with the overall block capacitance  $C_T$ . Now, if the ratio between a more advanced technology minimum length and the simulated 90-nm technology is  $\alpha$ , then the overall capacitance will vary as roughly  $\alpha^2$  for a constant aspect ratio.

The phase word as aforementioned in Section III is the truncated 8-bit word while the amplitude information must be coded at least with 9 bit. The size of the ROM is therefore about  $(2^8 \times 9)$  2304 bit, and a  $2^4 \times 2^8$  memory matrix is sufficient. Let us consider  $n - k = 4$  rows and  $k = 8$  columns.<sup>9</sup>

Following the work in [13], the ROM power consumption can be evaluated by considering all the different components involved in a single phase to amplitude conversion. The

<sup>9</sup> Particularly, for bigger ROMs, several optimization techniques can be used to reduce the ROM power consumption.

TABLE V  
PARAMETERS OF 90-NM CMOS TECHNOLOGY

PARAMETER	VALUE	UNIT
$C_{int}$	90 <sup>a</sup>	aF/ $\mu\text{m}$
$C_{tr}$	220	aF
$d_m$	1.45	$\mu\text{m}$
$V_{dd}$	1	V
$V_{swing}$	1	V
$W_{int}$	0.14	$\mu\text{m}$
$I_{sens}$	90	$\mu\text{A}$

<sup>a</sup>Minimum interconnection width equal to 0.14 $\mu\text{m}$

TABLE VI  
MEMORY-CELL EVALUATION POWER CONSUMPTION

Clock frequency [MHz]	Power consumption [ $\mu\text{W}$ ]
45	32.3
75	53.8
135	96.9

TABLE VII  
ROW-DECODING AND COLUMN-SELECT GLOBAL POWER CONSUMPTION

Clock frequency [MHz]	Power consumption [ $\mu\text{W}$ ]
45	5.5
75	9.1
135	16.4

power consumed by the  $2^k$  memory cells on a row during one precharge or evaluation can be approximated by the following:

$$P_{\text{memcell}} = \frac{2^k}{2} (c_{\text{int}} l_{\text{column}} + 2^{n-k} C_{\text{tr}}) V_{\text{dd}} V_{\text{swing}} \quad (16)$$

where  $P_{\text{memcell}}$  is the approximated power consumption of the ROM,  $c_{\text{int}}$  is the capacitance of a unit wirelength with minimum width,  $C_{\text{tr}}$  is the minimum-size gate capacitance,  $V_{\text{dd}}$  is the power-supply voltage, and  $V_{\text{swing}}$  is the voltage swing of each memory cell. Defining the memory cell as  $d_m \times d_m$  square, then the column interconnection length of the memory matrix is  $l_{\text{column}} = 2^{n-k} d_m$ .

Now, considering, as an example, the 90-nm CMOS technology, the parameters shown in Table V are available. With these values,  $P_{\text{memcell}} = 718$  fW/operation.

Concluding, the power consumption for the three different operating frequencies is given in Table VI.

The row-decoding-part power consumption is negligible, and therefore, it will not be considered. The power from row driving is given by [13]

$$P_{\text{rd}} = 0.5 \{ 2^{k+1} C_{\text{tr}} + 2(n-k) C_{\text{tr}} + c_{\text{int}} [8(n-k) W_{\text{int}} + l_{\text{row}}] \} V_{\text{dd}}^2 \quad (17)$$

while the column-select power consumption is given by

$$P_{\text{cs}} = \frac{1.3}{2} \left( \sum_{i=1}^{k-1} 2^{k-i} C_{\text{tr}} + k c_{\text{int}} l_{\text{column}} \right) V_{\text{dd}}^2 \quad (18)$$

where  $l_{\text{row}} = 2^k d_m$ . The power-consumption summary is given in Table VII.

TABLE VIII  
OVERALL PHASE-ACCUMULATOR AND ROM POWER CONSUMPTION

Clock frequency [MHz]	Power consumption [ $\mu\text{W}$ ]
45	167.8
75	212.9
135	299.3

The last contribution mainly comes from the sense amplifier. This contribution is equal to  $V_{\text{dd}} I_{\text{sense}}$ , and it is frequency-independent. The sense amplifier consumes approximately 90  $\mu\text{W}$  as can be derived from Table V. The overall ROM and accumulator power consumption for the three different operating frequencies is given in Table VIII.<sup>10</sup> At this point, it is possible to make an important observation. It is common to believe that, in a DDS, the ROM consumes most of the power. This is true for a high-demand DDS while, for a power-constrained DDS, the situation is different. Indeed, the highest power consumption for the digital DDS back-end is around 300  $\mu\text{W}$  and, therefore, far from commonly reported figure of some tens of milliwatts of high-end DDSs.

### C. DAC Power-Consumption Estimation

The last step consists in predicting the DAC power consumption with the reference clock frequency. The architecture choice is driven by reduction of the power consumption and the capability to handle the high-speed operations. The most common DAC architectures are the following:

- 1) oversampled  $\Sigma\Delta$ ;
- 2) R-2R;
- 3) charge redistribution;
- 4) current steering.

The oversampled DACs are mainly used to achieve high resolution at low frequencies ( $< 10$  MHz). Furthermore, they involve analog operations and can be very complex at high frequencies. For a relative high-frequency low-power DAC, a very efficient architecture is the R-2R or the charge-redistribution topologies. In these topologies, most of the current will be used (see Section IV-C1) only to drive the following stage (the AA filter) and not in the conversion itself.

1) *R-2R DAC*: There are two ways in which the R-2R ladder network may be used as a DAC, known, respectively, as the voltage and the current modes. They are shown in Fig. 3(a) and (b). In the voltage-mode R-2R ladder DAC, the ‘‘rungs’’ of the ladder are switched between  $V_{\text{ref}}$  and ground, and the output is taken from the end of the ladder. The voltage output is an advantage of this mode, as is the constant output impedance, which eases the stabilization of any amplifier connected to the output node. Additionally, the ladder’s branches switch between a low impedance  $V_{\text{ref}}$  connection and ground, so capacitive glitch currents tend not to flow in the load.

The main advantage of the current-mode topology is its speed because the input of the buffer is at virtual ground. The normal connection of a current-mode ladder-network output is to an OPAMP configured as current-to-voltage (I/V) converter, but stabilization of this OPAMP is complicated by the DAC output-

<sup>10</sup>By using simple logic functions, it is possible to use the same ROM for both sine and cosine generations. For this reason, the power consumption of a single ROM has been considered even if quadrature generation is required.

TABLE IX  
MAXIMUM DELAY TIME AND  $R$  VALUE FOR THE R-2R LADDER

Operating frequency [MHz]	Max Delay [ns]	$R_{\max}$ [k $\Omega$ ]	Power Consumption [ $\mu$ W]
45	11	18	12
75	6.5	11	18
135	3.5	6	34

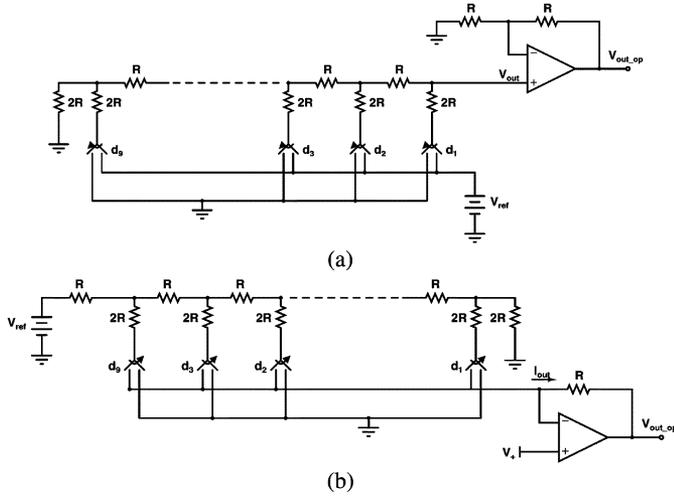


Fig. 3. R-2R DAC topologies. (a) Voltage-mode R-2R DAC. (b) Current-mode R-2R DAC.

impedance variation with digital code. Of course, capacitive glitches are larger for the current-mode topology with respect to the voltage mode. Glitches create an unwanted harmonic distortion during waveform generation, and therefore, a voltage-mode topology is used. Consequently, also the AA filter will be supposed to work in voltage mode. In an R-2R DAC, there are three main sources of power consumption:

- 1) R-2R resistive chain;
- 2) output buffer;
- 3) switch drivers.

The power consumption of the resistive ladder can be derived by using the following formula [14]:

$$P_j = \sum_{i=1}^n d_i I_i V_{ref} \quad (19)$$

where  $j$  refers to the  $j$ th digital code considered,  $V_{ref}$  is the DAC reference voltage,  $d_i$  ( $i = 1, 2, \dots, n$ ) is the  $n$ -bit binary number to be converted into the analog voltage, and  $I_i$  is the current flowing through each leg of the resistive chain, and it is given by the following:

$$I_1 = \frac{d_1 V_{ref} - V_{out}}{2R} \quad (20)$$

$$I_{i|(i=2,3,\dots,n+1)} = \frac{d_i V_r - \left[ V_{out} - R \sum_{k=1}^{i-1} (i-k) I_k \right]}{2R} \quad (21)$$

where  $d_{n+1} = 0$  and  $V_{out}$  is the output voltage of the DAC and it is equal to

$$V_{out} = (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \times V_{ref} \quad (22)$$

The power consumption of the R-2R ladder is a function of the input code. Now, supposing that the probability that a certain code is addressed is equal for all the codes, then the rms power dissipation can be calculated using the following:

$$P_{rms} = \frac{1}{N_{code}} \times \sum_{j=1}^{N_{code}} P_j \quad (23)$$

where  $N_{code}$  is the total number of codes in the DAC (e.g., for a 9-bit DAC, it equals  $2^9 - 1$ ). As can be seen from (20), (21), and (23), the power consumption depends on the resistance value  $R$ . At each node of the R-2R ladder shown in Fig. 3(a), there will be a parasitic capacitance due to interconnections and junctions. Furthermore, the input of the operational amplifier is not at virtual ground as it would have been in the case of a current-mode R-2R topology. This means that, between the time at which the digital word is set and the time at which the converted voltage will be available at the input of the output buffer, there will be a delay caused by the buffer input capacitance. This delay should not exceed 50% of the time available for a single conversion, and it depends on the DDS operating frequency.

The maximum delay time and maximum value of  $R$  in the three different cases are shown in Table IX. The values have been derived via simulations. The resistance value has been derived through simulation of the same ladder, including the parasitics at the internal nodes. In the same table, the power consumption of the R-2R ladder in the three possible cases is also shown.  $V_{ref}$  has been considered equal to 0.5 V.<sup>11</sup>

Another limit to the maximum value of resistance in the ladder comes from noise considerations. Indeed, the noise added by the chain-equivalent resistance and the feedback resistances must fulfill the required SNR specification. From (6), given a 9-bits DAC, the SNR is 51 dB when only the quantization noise is considered. It is desirable that all other noise sources are at least 6 dB below the quantization noise. Therefore, the SNR, when the noise of the OPAMP and one of the resistive ladders is considered, should be 57 dB. Supposing that the two contributions are equal, each of them must account for the overall noise so that their SNR is 60 dB. Supposing to have the noise from resistances 60 dB below the signal level which has a peak value  $V_{peak}$ , the following holds:

$$\frac{V_{peak}^2}{12kTRf_{max}} \geq 10^6 \quad (24)$$

where  $k$  is the Boltzmann constant and  $T$  is the temperature in degrees Kelvin. From the previous equation, the resistance value has to be smaller than 83 k $\Omega$  (with  $V_{peak} = 0.25$  V) which is in line with the values in Table IX.

<sup>11</sup>The noninverting configuration of the OPAMP has a gain equal to two.

TABLE X  
TYPICAL FILTER RESISTANCE, FILTER INPUT CAPACITANCE, AND DAC BUFFER CURRENT CONSUMPTION VERSUS FREQUENCY

Clock frequency [MHz]	Max filter resistance [k $\Omega$ ]	AA-Filter input capacitance [pF]	Buffer Power consumption [ $\mu$ W]
45	12	0.89	336
75	28	0.38	144
135	42	0.19	72

TABLE XI  
PARAMETERS OF 90-NM CMOS TECHNOLOGY

Parameter	Value	Unit
$C'_{ox}$	7.8	$\frac{fF}{\mu m^2}$
$\mu_n$	200	$\frac{cm^2}{Vs}$
Early Voltage $V_A$	2.75	V

The output buffer of the DAC needs to drive the input impedance of the following stage (the AA filter). The filter for the three different cases (different image position) can be designed by using standard software tools. These tools require generally a typical resistor value. Of course, the value of this resistor will set the required capacitance and, ultimately, the input capacitance of the filter. The maximum resistor value can be derived from noise considerations. The filter must contribute negligibly to the overall noise. Therefore, having set earlier the DAC SNR to 51 dB (the system is spurs-dominated) and because no gain is achieved up to the AA-filter input, it is desirable to have the noise floor of the filter 6 dB below the required SNR. Therefore, an SNR of 57 dB is a good choice. Now, from [15]

$$\frac{V_{rms,sig}^2}{V_n^2} = \frac{V_{rms,sig}^2}{4kT \times nR\xi \times BW} \quad (25)$$

where  $V_{rms,sig}^2$  is the rms signal value,  $V_n^2$  is the noise power,  $n$  is the filter number of poles,  $R$  is the typical resistor value,  $\xi$  is the excess noise factor, and  $BW$  is the filter bandwidth. The maximum resistance value and filter input capacitance for the three different frequencies are given in Table X.

For the OPAMP, in the output buffer, a gain of 100 would be required to avoid nonidealities coming from the amplifier finite gain. All the parameters required for the evaluation of the buffer power consumption for the CMOS 90-nm technology are listed in Table XI. To reduce the current consumption, it is reasonable to drive the transistors in weak inversion. Given the required voltage gain  $A_{V0}$ , the minimum channel length to achieve this gain with a single-stage amplifier is given by the following [16]:

$$L = \frac{n\phi_t A_{V0}}{V_A} \frac{1 + \sqrt{1 + i_d}}{2} \quad (26)$$

where  $\phi_t$  is the thermal voltage roughly equal to 25 mV,  $n$  is the slope factor ( $n \simeq 1.6$  in weak inversion),  $V_A$  is the Early voltage, and  $i_d$  is the inversion coefficient (between 0.1 and 1 in weak inversion). Considering an inversion coefficient equal to 0.5, the required transistor channel length for a gain of 100 is equal to 1.62  $\mu$ m.

Now, the relation between current and gate-source voltage in a MOS transistor is given by the following relation:

$$I_{DS} = \frac{1}{2} \mu_n C'_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (27)$$

where  $\mu_n$  is the electron mobility,  $C'_{ox}$  is the gate capacitance per unit area,  $W$  is the transistor width,  $L$  is the channel length, and  $V_{GS} - V_T$  is the overdrive voltage.

Now, it can be proven [17] that the bandwidth of an amplifier can be expressed as a function of the bias current by the following:

$$BW = \frac{3 \cdot I_{DS}}{2\pi \cdot (V_{GS} - V_T) \cdot C'_{ox} WL} \quad (28)$$

The inversion coefficient  $i_d$  [18] can also be expressed as a function of the bias current with the following:

$$i_d = \frac{I_{DS}}{2n \cdot \mu_n C'_{ox} \frac{W}{L} \cdot \phi_t^2} \quad (29)$$

Now, from (27), (28), and (29), the maximum achievable bandwidth can be expressed as a function of the channel length

$$BW = \frac{3}{2\pi} \sqrt{n i_d} \frac{\mu_n \phi_t}{L^2} \quad (30)$$

From (30), substituting all the known values and a channel length of 1.62  $\mu$ m, a maximum achievable bandwidth of 81 MHz is obtained. This proves that a single-stage amplifier can achieve, at the same time, the required speed and gain given the required bandwidth of 15 MHz.

The minimum bias current to achieve the required specifications is given by the following [16]:

$$I_{DS} = n\phi_t (2\pi GB C_L) \quad (31)$$

where GB is the gain-bandwidth product and  $C_L$  is the load capacitance. The buffer-estimated power consumption for the three different frequencies is given in Table X.

To avoid performance degradation in the DAC, the switch on-resistance has to be much lower than the 2R value in the R-2R ladder. The actual required resistor matching can be derived by the following [19]:

$$T \leq \frac{INL}{0.577 \times 2^N} \quad (32)$$

where  $T$ , as defined in [19], is the resistor tolerance. This contribution comes from both the actual resistor and the switch resistance. Given the fact that they are stochastically independent, they sum in a quadratic form, and if we suppose their contribution as equal, then  $\Delta R_{TOT} = \sqrt{2} \Delta R_{SW}$ , where  $\Delta R_{TOT}$  and  $\Delta R_{SW}$  are the maximum allowed variance in a single ladder branch and the variance of the switch resistance, respectively. In this way, supposing a  $\pm 30\%$  mismatch in the transistor on-resistance, the maximum resistance value can be calculated for the LSB switch for the three different operating frequencies (see Table XII).

TABLE XII  
SWITCH PARAMETERS

Frequency [MHz]	$R_{\text{on}}^{\text{max}}$ [ $\Omega$ ]	W·L [ $\mu\text{m}^2$ ] <sup>a</sup>	Gate capacitance ( $C_{\text{SW}}$ ) [fF]
45	360	1.04	13.2
75	220	1.6	21.7
135	120	3.0	40.5

<sup>a</sup>All switches are considered minimum length.

TABLE XIII  
TIME CONSTANTS, MAXIMUM DRIVER LOAD RESISTANCE, LSB CURRENT, AND OVERALL POWER CONSUMPTION FOR DIFFERENT DAC OPERATING FREQUENCIES

Frequency [MHz]	Max time constant ( $\tau_{\text{max}}$ ) [ns]	$R_L^{\text{max}}$ [k $\Omega$ ]	$I_B^{\text{LSB}}$ [ $\mu\text{A}$ ]	$P_{\text{TOT}}$ [ $\mu\text{W}$ ] <sup>a</sup>
45	2.2	83.5	10.8	97.2
75	1.3	30	30	270
135	0.74	9.2	98.4	886

<sup>a</sup>At  $V_{\text{supply}} = 1\text{V}$

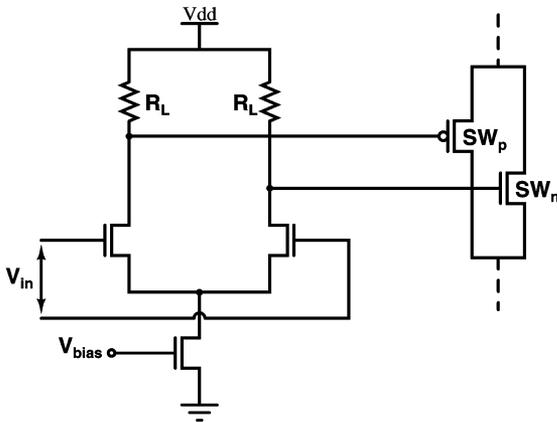


Fig. 4. Switch driver schematic.

A very common transistor-level implementation of a CMOS switch, together with the driving circuit, is shown in Fig. 4.<sup>12</sup> The driver should be able to switch the gate transistors on and off very rapidly. Therefore, the transition edges have to be very sharp. This means that the time constant at the gate of the n-MOS transistor ( $SW_n$ ) and p-MOS transistor ( $SW_p$ ) must be very small as compared to the DAC sample time. Considering a ratio of ten between the DAC sample time and the switching time for the LSB, Table XIII summarizes the maximum  $RC$  time constant at the switch gate and, therefore, the maximum load resistance  $R_L$  for the various DAC operating frequencies.

At this point, the driver must be able to switch its voltage outputs between  $V_{dd}$  (when in one of the branches no current is flowing) and  $2 \times (V_{GS} - V_{TH}) \simeq 0.1\text{V}$  to allow the current source transistor shown in Fig. 4 to work in saturation. Considering a 1-V power supply, the driver has a peak-to-peak voltage swing of about 0.9-V single-ended. Therefore, the required dc current for the LSB switch driver is simply given by  $I_B^{\text{LSB}} = (V_{\text{swing}})/(R_L^{\text{max}})$ , and the values for the three different frequencies are given in Table XIII. The time constant at the

<sup>12</sup>Although it could be argued that simple inverters and buffers can be used as driving stages, it should be noticed that, for linearity reasons, this is not a common practice. Furthermore, the proposed driving stage does not hit the supply, which constitutes another advantage of this configuration with respect to simple inverters or buffers when linearity is considered.

input of the switch is roughly given by  $R_L \times 2C_{\text{SW}}$ ,<sup>13</sup> where  $C_{\text{SW}}$  is given in Table XII for the three different frequencies.

The total current consumption for all drivers is  $9 \times I_B^{\text{LSB}}$ . The drivers' current consumption for the three different DAC operating frequencies is given in Table XIII.

2) *Charge-Redistribution DAC*: The resistive ladder can be replaced by a capacitive ladder in which the resistance  $R$  is replaced by a capacitance  $2C$  and the resistance  $2R$  by a capacitance  $C$ . This architecture has a big advantage in terms of both area and power consumption over the common weighted-capacitance architecture as shown in [20]. This topology has, as main advantage over the R-2R architecture, the fact that no DC current is flowing. Indeed, the energy consumption only takes place during charging or discharging cycles. On the other hand, capacitive dividers are sensitive to stray capacitances which can heavily affect the accuracy.

In [20], it has been shown that, on silicon substrate, because of the bottom-plate parasitic capacitance, it is impossible to realize even a 4-bit C-2C DAC. Therefore, a simpler weighted sum architecture has to be used, but as stated before, the power consumption becomes comparable with a common R-2R architecture without any other advantage.

## V. RESULTS

From Fig. 2, the overall DDS power consumption for a quadrature output is given by the following relation:

$$P_{\text{DDS}} = P_{\text{dig}} + 2 \times P_{\text{DAC}} + 2 \times P_{\text{AA}} \quad (33)$$

where  $P_{\text{dig}}$  is the digital back-end power consumption,  $P_{\text{DAC}}$  is the DAC power consumption, and  $P_{\text{AA}}$  is the AA-filter power consumption. The power consumption of the digital blocks versus the operating frequency is shown in Fig. 5. As expected, the overall power consumption grows roughly linearly with the reference clock frequency.

The DAC power consumption is shown together with the power consumption of its building blocks in Fig. 6. As shown, the R-2R ladder power consumption is negligible. A minimum in the overall DDFS power consumption is located around 100 MHz (see Fig. 8). On the left side of the minimum, the power is

<sup>13</sup>The factor two takes into account that we need two switches per branch because each branch can be switched either toward  $V_{\text{ref}}$  or ground.

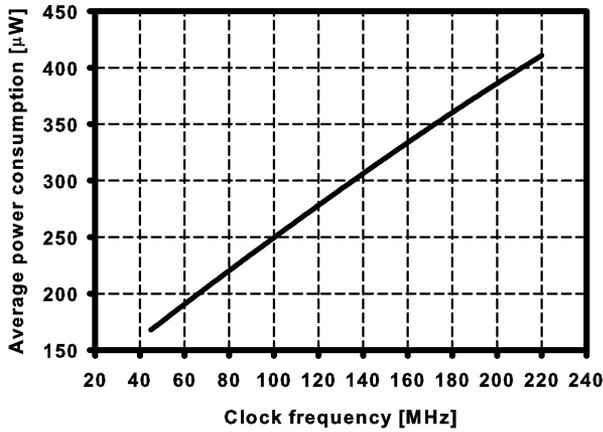


Fig. 5. Digital back-end power consumption versus reference clock frequency.

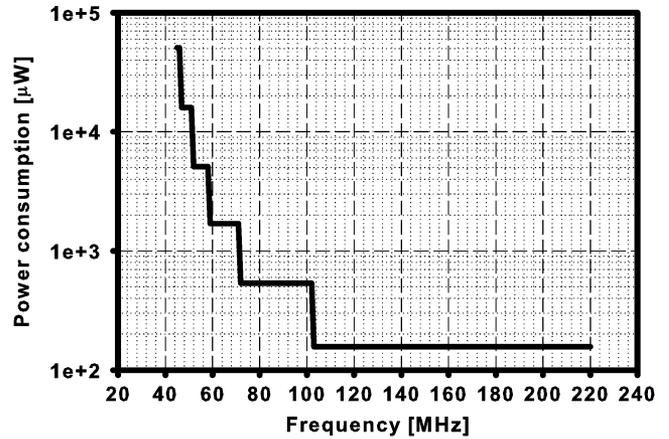


Fig. 7. AA-filter power consumption.

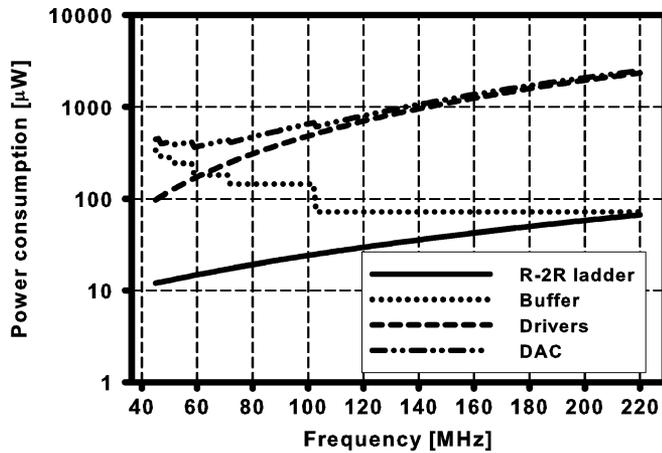


Fig. 6. DAC power consumption.

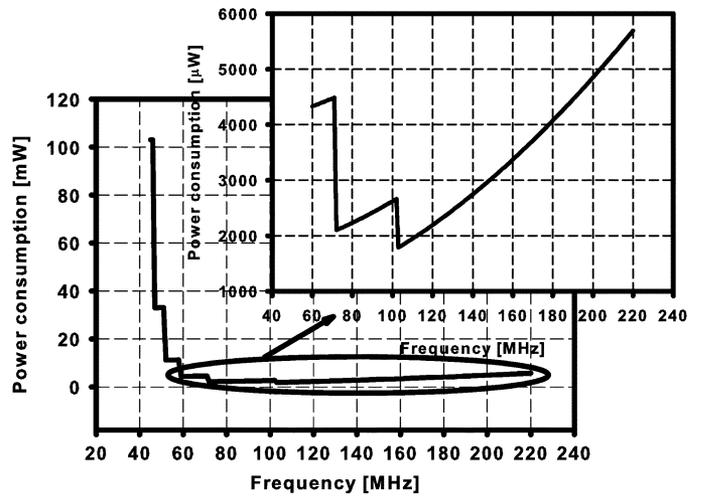


Fig. 8. DDS power consumption.

dominated by the output buffer. Indeed, lowering the reference frequency requires an increase in the filter order, and consequently, the filter input capacitance grows. As a consequence, the output buffer bias current needs to increase. The power consumption of the output buffer has a typical staircase structure due to the fact that a given filter order fulfills the requirements in terms of image attenuation for a certain range of frequencies. On the right side of the optimal reference frequency, the overall power consumption is dominated by the switch drivers.

The filter power consumption is shown on a logarithmic scale in Fig. 7, while the overall power consumption is shown in Fig. 8. A minimum is located at around 100 MHz. On the left side, the filter will dominate the overall power consumption, while on the right side, the drivers in the DAC are again the most power-hungry blocks.

The minimum power consumption is around 1.8 mA for the complete DDS system. Given the 103-MHz reference clock frequency, the power-consumption breakdown is shown in Fig. 9. The most power-hungry blocks are the DACs with almost 70% of the overall power consumption.

The attenuation of the image frequency due to the sinc function has been derived in Section III, considering an initial reference frequency of 40 MHz. Now, with the new reference frequency, it is possible to recalculate this value to check if it is possible to reduce the filter order. If this would be the case,

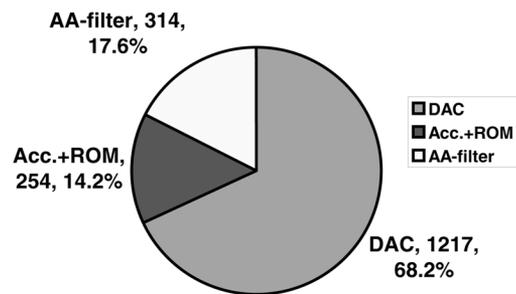


Fig. 9. Power-consumption breakdown by block (power in microwatts).

the overall procedure needs to be repeated iteratively until convergence.

The extra attenuation due to the sinc function with respect to the 40-MHz case is only 1.34 dB and, therefore, not enough to reduce the number of poles in the filter from the optimal value of two poles. Concluding the previously calculated optimal number of poles is still valid.

In Fig. 10, the minimum power consumption versus the SFDR is shown. In the same graph, the optimal reference frequency is also shown. It is shown that there are two trends. Below around

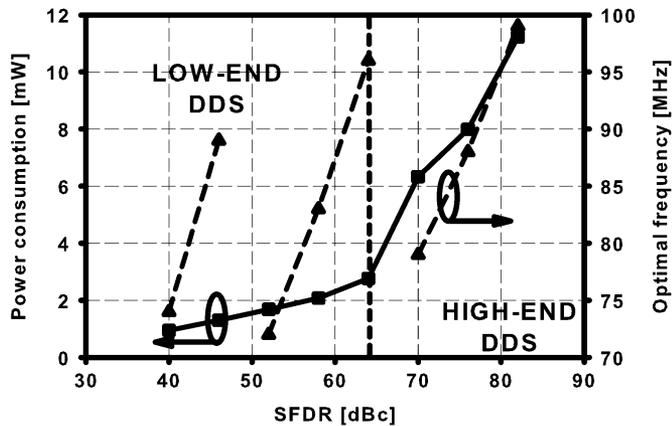


Fig. 10. Minimum power consumption and optimal reference clock versus SFDR.

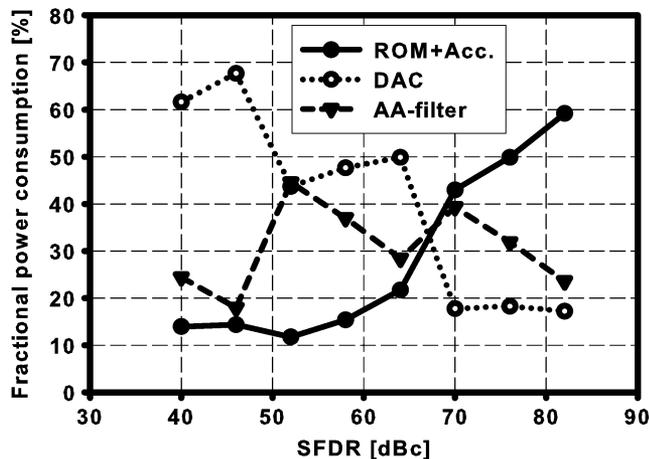


Fig. 11. Power-consumption breakdown versus SFDR.

64-dBc SFDR, the system is dominated in terms of power consumption by the analog part (DAC+AA filter). The power increases with a slope which is lower than in the case of an SFDR above 64 dBc. This can be explained with the fact that the maximum operating frequency is always constrained to 15 MHz, and the DR of the filter has been kept constant (58 dB)<sup>14</sup>. The increment is due mainly to an increase in the filter requirements and in the digital back-end. Above 64 dBc of the SFDR, the digital back-end starts to consume most of the power due to the huge increment in the ROM size. Therefore, in the right area, the power consumption is dominated by the digital back-end.<sup>15</sup> This area is the area of the high-end DDS.<sup>16</sup> In the area of high-end DDS, all the choices made in this paper can be not more valid and a better solution has to be found for power optimization. To

<sup>14</sup>Getting a high DR from an analog block can cause a sensible increase in the power consumption. Therefore, if the digital back-end is designed for higher SFDR (the cost in terms of power consumption to obtain this requirement is decreasing with technology scaling), it is possible to conceive a dedicated pre-distortion algorithm or a notch filter to cancel or reduce the harmonic distortion of the analog filter without using the brute-force approach (increase the power consumption)

<sup>15</sup>The phase accumulator has a constant power consumption. Its size depends only on the required resolution and reference clock frequency.

<sup>16</sup>The DAC required number of bits in this area is above 12. Therefore, to still keep the same DAC topology, a laser trimming of the resistances or a calibration loop are required.

further confirm these results, the power breakdown versus the SFDR is shown in Fig. 11. The crossing point of 64 dBc is the point at which the power consumption of the digital back-end exceeds the power consumption of the analog components and sets the new trend in the overall power consumption. As already known from literature at high SFDR, the power consumption is dominated by the ROM power consumption, and the previous graphs confirm these rule.

## VI. CONCLUSION

Ultralow-power FH systems require a different approach in terms of system and circuit design. Conceiving a system which has the lowest possible requirements while still achieving a good communication range and a robust link is a must in order to minimize the overall power consumption. In this framework, it is crucial to develop a power-estimation model that can predict the power-consumption limit for the hopping synthesizer, which results to be the most demanding block in terms of power consumption.

Different from the general belief that the digital back-end dominates the power consumption, this paper proves that, for low-end DDS (SFDR < 64 dBc) systems suitable for low data-rate applications, the bottleneck in the power consumption is the analog part with more than 40% of the power used in the DAC.

This model predicts a minimum power consumption of about 1.8 mW from a 1-V power supply for an SFDR of 46 dBc, mainly used in the DAC output buffer (68%). In this sense, the model helps the designer in estimating how much power the DDS system requires without any design effort and can be extended to DDS with tighter specifications for high-end applications.

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