

A 9.8–11.5-GHz Quadrature Ring Oscillator for Optical Receivers

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Abstract—This paper describes a quadrature ring oscillator that is tunable from 9.8 to 11.5 GHz in a 30-GHz f_T BiCMOS technology. The ring oscillator can be used in advanced data clock recovery architectures in optical receivers. The circuit implementation of the oscillator uses transistors as active inductances. Isolation between the oscillator and cascaded circuits, such as buffers and flip-flops, is improved by utilizing the active inductances in a cascode configuration. Carrier to noise ratios better than 94 dBc/Hz at 2-MHz offset are measured with 75-mW dissipation and 2.7-V supply voltage. The evolution in two-stage ring oscillator topologies, leading to the realized design, is discussed in detail on the circuit level.

Index Terms—Bipolar transistor oscillators, clock and data recovery, optical communication, oscillators, phase noise.

I. INTRODUCTION

IN DATA transmission over optical fibers, one of the key functions of the receiver front end is data clock recovery (DCR). In networks following the synchronous optical network (SONET) standard or the synchronous digital hierarchy (SDH) standard, nonreturn-to-zero (NRZ) data signals are used. The task of the DCR circuit is to extract the clock information from the NRZ data. This means that the DCR circuit must be able to acquire phase lock with the clock signal from the random data.

Many advanced integrated DCR circuits are phase-locked-loop (PLL) based [1]. Since the free-running frequency of the oscillator in the PLL is never exactly the same as the incoming data rate, the DCR circuit must obtain frequency lock prior to phase lock. In practice, this means that every PLL-based DCR circuit needs some type of frequency acquisition aid [1]. One possibility is to use a crystal oscillator to keep the oscillator frequency within the acquisition range of the PLL, but this solution requires an expensive external crystal and an IC pin. Fully integrated solutions have been realized in which the DCR architecture has a frequency discriminator as an integral part of the architecture [2]. This requires an oscillator which provides quadrature (I/Q) signals. The availability of quadrature signals also allows the construction of half-rate DCR architectures [3]. Half-rate DCR circuits operate at half the frequency of the incoming data rate.

This paper presents an investigation of three I/Q ring oscillator topologies for 10-Gb/s DCR circuits which require quadrature signals. The SONET standard OC-192 (equivalent to SDH STM-64) requires clock extraction at a bit-rate of

TABLE I
SHORT LIST OF THE SPECIFICATIONS OF THE DCR RING OSCILLATOR

Specification	Value	Unit
Technology	BiCMOS 30 GHz f_T	
Frequency	9.953280	GHz
CNR(2 MHz)	95	dBc/Hz
Power budget	100	mW
Power supply voltage	2.7	V
Tuning input	Differential	
Output(s)	In-phase / Quadrature	

9953.28 Mb/s (~ 10 Gb/s). The target specifications for the quadrature oscillator are shown in Table I and have been derived from DCR system considerations and simulation. The power budget of 100 mW is based on the knowledge that a ring oscillator will be used rather than an LC oscillator. Compared to an LC oscillator, a ring oscillator needs a higher level of power dissipation to meet the carrier-to-noise ratio (CNR) of 95 dBc/Hz at 2-MHz offset.¹ However, the CNR specification required for DCR circuits is orders of magnitude lower compared to, for example, local oscillator requirements in wireless front ends, which makes the use of ring oscillators feasible in DCR systems. In particular, the compact chip area and the, in general, large tuning range of a ring oscillator, make it a good candidate for use in DCR circuits.

A key aspect of the presented ring oscillator topology study is the technology used to investigate the performance of the oscillators. As shown in Table I, a BiCMOS technology is specified with a 30-GHz transition frequency (f_T) [4]. Constructing a quadrature ring oscillator with a CNR (2 MHz) of 95 dBc/Hz at 1/3 of the f_T with less than 100-mW dissipation is a design challenge. The combination of the oscillation frequency, CNR, and dissipation target and technology has led to the presented evolution of ring oscillator circuits. The influence of the parasitics is dominant at 10 GHz, and circuit complexity must be low. Every additional device will add device and interconnect parasitics, which reduce the oscillation frequency and the carrier level.

Three two-stage ring oscillators are discussed on the circuit level in Section II. The most promising ring oscillator implementation employs stacked active inductances. Section III explains how the active inductances in this ring oscillator can be utilized to improve the isolation between the oscillator core and cascaded circuits. The experimental results of the quadrature oscillator with stacked active inductances are discussed in Section IV, and compared with other reported ring oscillators in Section V.

¹This frequency-domain specification is derived from the time-domain OC-192 specification assuming the oscillator is part of a PLL with a loop bandwidth of 10–12 MHz.

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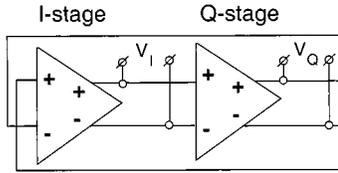


Fig. 1. Block diagram of a two-stage quadrature oscillator.

II. TWO-STAGE RING OSCILLATOR TOPOLOGIES

The oscillation frequency and CNR specification are the primary objectives for the DCR ring oscillator design. The large-signal oscillation frequency in a ring oscillator is equal to $(2N\tau_{\text{delay}})^{-1}$, in which N is the number of stages and τ_{delay} the large-signal delay of a stage. A two-stage ring oscillator is, therefore, most interesting as a starting point for the DCR oscillator design, since it has the highest frequency and provides I/Q signals. Two stages are also the optimum number of stages concerning phase noise minimization. Analysis of differential ring oscillators with a time-variant phase noise model shows that a minimum number of ring oscillator stages is optimum [5]. It is more efficient to invest power in two stages compared to spending part of the power budget in additional stages. Doubling of the power and reducing all impedance levels by a factor of 2 in an oscillator immediately gives 3-dB CNR improvement.

A block diagram of a two-stage ring oscillator is shown in Fig. 1. The model consists of two identical sections and one inversion, and the phase condition for oscillation dictates a 90° phase shift per section. Therefore, a two-stage oscillator with identical stages provides “correct-by-construction” I/Q signals on the behavioral level. Practical I/Q matching is limited by device matching and layout symmetry.

In Section II-A, three implementations of the stages in Fig. 1 are discussed. Oscillation frequency maximization is used as a criterion to select the most promising topology. The circuit implementation with the maximum oscillation frequency (above 10 GHz) will have the highest gain and signal swing at the (lower) target frequency of 10 GHz, which will result in better CNR figures. The qualitative discussion in Section II-A is followed by a quantitative analysis of the three oscillator implementations in Section II-B, in which the maximum oscillation frequency of the topologies in a 30-GHz f_T BiCMOS process is determined by an automatic circuit optimizer.

A. Three Circuit Implementations

A potential circuit solution for the realization of the DCR oscillator is the two-integrator oscillator [6]. The circuit diagram of one stage of this oscillator (the stages in Fig. 1 are identical) is shown in Fig. 2(a). Maximum oscillation frequency is obtained when lumped capacitor C_1 is omitted. In that case, the integration capacitance in each section consists completely of parasitic capacitance. A realization of the two-integrator oscillator in an 11-GHz f_T BiCMOS process has been reported for use in digital satellite receivers [6]. This design had a wide tuning range (0.9–2.2 GHz) and achieved a CNR (2 MHz) of 106 dBc/Hz with an oscillator core dissipation of 100 mW. However, simulations of this circuit in the specified 30-GHz f_T BiCMOS

process, revealed poor CNR levels at 10 GHz. Furthermore, the parasitic phase shift of the differential pairs in the circuit prevent oscillation beyond 10.3 GHz. The performance limits imposed by the technology prevent further improvement. Hence, a topological change is needed in order to achieve a higher maximum oscillation frequency and better CNR.

A promising option to extend the oscillation frequency and improve the CNR is to alter the circuit in Fig. 2(a), such that the parasitic phase shift of transistors Q_{T1} and Q_{T2} is partly compensated. Interestingly, only a small topological change in Fig. 2(a) is needed to realize this. If the transistors Q_{A1} and Q_{A2} in Fig. 2(a) are connected with shorted base and collector to the collectors of Q_{T1} and Q_{T2} , the oscillator circuit in Fig. 2(b) is obtained [7]. For high frequencies, a transistor with shorted base and collector implements an active inductance, and implements effectively inductive peaking which extends the oscillation frequency of the oscillator [7]. This circuit will be referred to as the ring oscillator with folded active inductances. Tuning is realized by varying the bias current I_{tune} of transistors Q_{L1} and Q_{L2} , which changes the inductance value.

The oscillation frequency of the ring oscillator with folded active inductances will be maximized if the parasitic capacitance seen at the collectors of transistors Q_{A1} and Q_{A2} in Fig. 2(b) is minimized. In the oscillator stage [Fig. 2(b)], the collector–substrate capacitance of transistors Q_{L1} and Q_{L2} adds to the total parasitic capacitance seen at the collectors of Q_{A1} and Q_{A2} . This contribution is eliminated when stacking the active inductances as shown in Fig. 2(c). However, the current through transistors Q_{A1} and Q_{A2} in Fig. 2(c) ($I_{\text{level}}/2$ in balanced condition) is now reused in transistors Q_{L1} and Q_{L2} . Therefore, a means of frequency control is needed in order to set the carrier level and frequency independently. This is realized with variable resistors $R_{\text{tune}1}$, $R_{\text{tune}2}$, which control the inductance value of Q_{L1} and Q_{L2} [8].

B. Simulation of the Maximum Oscillation Frequency

In order to quantify the maximum small-signal oscillation frequency of the three ring oscillator topologies, an automatic circuit optimizer was used. All transistors were modeled with the MEXTRAM transistor model [9] to include all high-frequency parasitics effects. The optimization goal was simply to maximize the oscillation frequency. All currents and resistor values were given as design parameters. The oscillation frequency was simulated using transient analysis and the value of the oscillation frequency was fed back to the optimizer, which adjusted the design parameters until a maximum value of oscillation frequency $f_{\text{osc|max}}$ was reached. It was needed to specify a minimum amplitude (~ 20 mV) as a constraint for the optimizer. The small-signal oscillation frequency is always higher than the oscillation frequency for a large signal swing. Therefore, the optimizer tries to find the highest frequency for which Barkhausen’s oscillation criteria are met, and minimizes the oscillation amplitude. The minimum signal constraint prevented the oscillation from stopping and causing convergence problems.

The results of the optimization are shown in Table II. As expected, the ring oscillator with stacked active inductances achieves the highest (small-signal) oscillation frequency. In

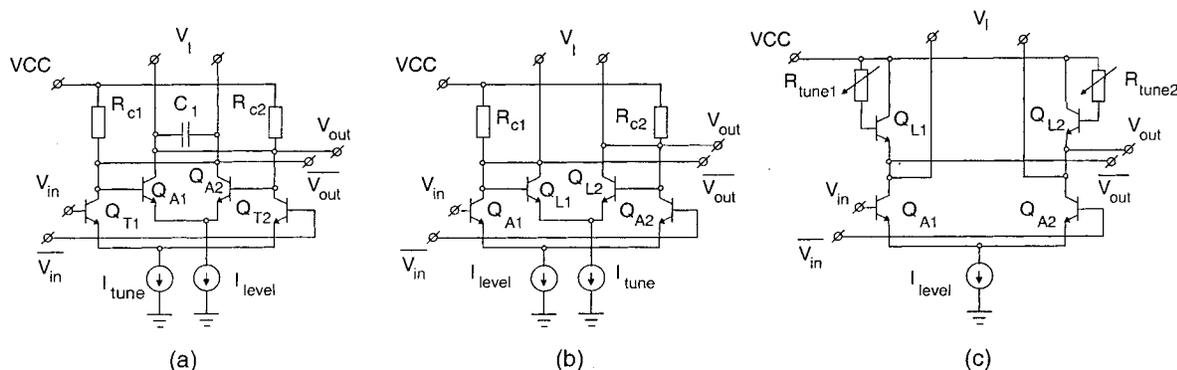


Fig. 2. Evolution in oscillator stage topologies. (a) A stage of a two-integrator oscillator implementation. (b) A stage with folded active inductances. (c) A stage with stacked active inductances.

TABLE II
MAXIMUM OSCILLATION FREQUENCY $f_{osc|max}$ OF THE THREE I/Q RING
OSCILLATOR TOPOLOGIES

Oscillator	Figure	$f_{osc max}$ [GHz]	$\frac{f_{osc max}}{f_T}$
Two-integrator	Fig. 2(a)	10.3	0.34
Folded inductances	Fig. 2(b)	13.5	0.45
Stacked inductances	Fig. 2(c)	20.2	0.67

practice, $f_{osc|max}$ is lower since interconnect capacitance is not taken into account.

The simulation results listed in Table II are obtained without loading the ring oscillators by, for example, buffers. Prior to realization of the ring oscillator with stacked active inductances, loading of the circuit by cascaded circuits has to be addressed. Minimization of these loading effects will be considered next.

III. ADDING BUFFERED OUTPUTS

The quadrature ring oscillator will be used in a DCR architecture. Therefore, buffers, flip-flops, or other circuits will be loading the ring oscillator. If these circuits are connected to the collectors of transistors Q_{A1} and Q_{A2} in Fig. 2(c), their contribution to the total parasitic capacitance can significantly lower the oscillation frequency. This loading effect can be reduced by providing alternative output terminals, which are isolated from the collectors of Q_{A1} and Q_{A2} .

Fig. 3(a) shows the half circuit of Fig. 2(c). The collector of transistor Q_{L1} is connected to V_{CC} with resistor R_L . This creates a buffered output node. For small values of R_L , the inductance of Q_{L1} remains practically unchanged when this resistor is added. Transistor Q_{L1} is now used for two functions. First of all, it implements the active inductance, and secondly, it provides cascode buffering.

The simulated buffered and unbuffered output signals [$V_{buffered}$ and $V_{unbuffered}$ in Fig. 3(b)] of the oscillator in Fig. 2(c) with collector resistors R_L inserted between the collectors of Q_{L1} , Q_{L2} , and V_{CC} , are shown in Fig. 4. The tail current I_{level} [see Fig. 2(c)], was set to 12 mA, which resulted in a large-signal oscillation frequency around 10 GHz. Resistor R_L was set to 20 Ω . The simulation results in Fig. 4 are obtained without loading the oscillator and performed at a maximum oscillation frequency of 11.6 GHz. The influence of

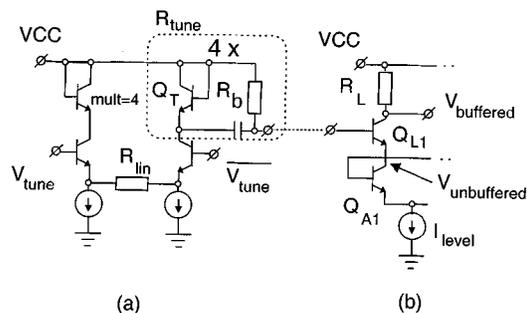


Fig. 3. Circuit implementation of the V/I -converter. (a) With differential tuning inputs and the half circuit of one oscillator section from Fig. 2(c). (b) With the active inductance (Q_{L1}) utilized as cascode stage.

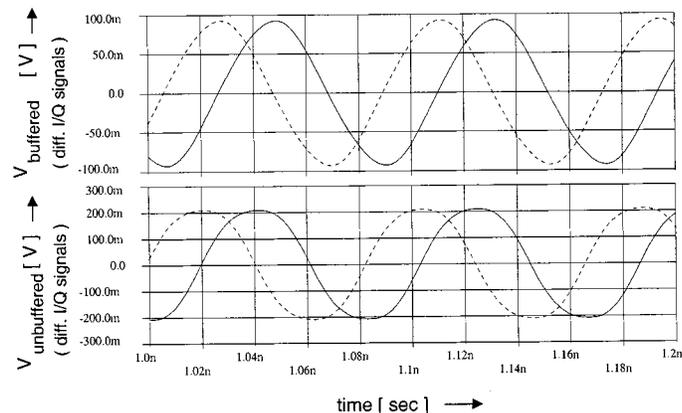


Fig. 4. Simulated differential quadrature signals at the buffered and unbuffered output terminals.

loading effects was investigated by connecting two differential pairs with 12-mA tail current (the same current level as the oscillator) to the collectors of Q_{A1} and Q_{A2} in Fig. 2(c). The simulated frequency dropped from 11.6 to 9.2 GHz and the output voltage, which was 216 mV_{peak} in Fig. 4, dropped to 101 mV_{peak}. On the other hand, the internal signal swing of the oscillator was 9 mV lower, and the oscillation frequency changed only 100 MHz, if the differential pairs were connected to the collectors of the stacked active inductances [Q_{L1} and Q_{L2} in Fig. 2(c)] with added collector resistors R_L . These simulation results illustrate the effectiveness of the output configuration shown in Fig. 3(b).

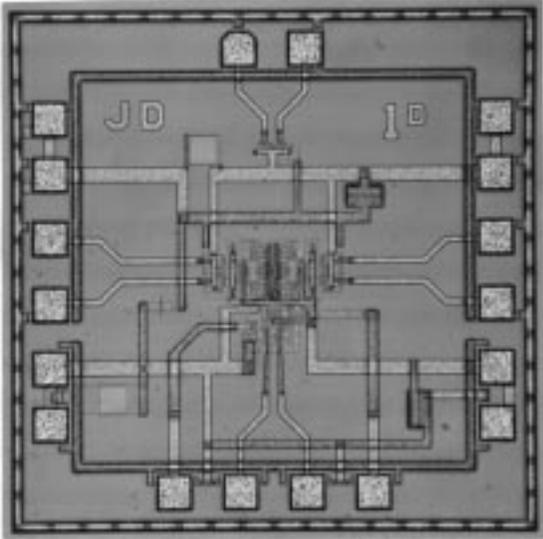


Fig. 5. Micrograph of the realized ring oscillator.

Fig. 3(a) shows the implementation of R_{tune} . To realize the variable resistance, diode-connected transistor Q_T is used, which is ac coupled to the base of the active inductance. Resistor R_b provides the base current for Q_{L1} . The current of transistor Q_T is controlled by a linearized differential pair. This implements differential tuning inputs.

The CNR of the quadrature oscillator constructed with the stage shown in Fig. 2(c), complete with the V/I converter shown in Fig. 3(a) and with R_L added to have buffered outputs, has been simulated with spectreRF. At 10 GHz, the simulated CNR is 95.3 dBc/Hz. The noise contribution of transistor Q_A (four in total, since there are two stages) is a dominant source ($4 \times 7.25\%$), followed by the active inductance Q_L ($4 \times 5.6\%$). Other contributors are the implementation of tail current source I_{level} ($2 \times 3\%$), the base resistance of Q_A ($4 \times 2.2\%$), and a multitude of other small noise sources. The tunable resistors R_{tune} , implemented by the boxed circuit [Fig. 3(a)], each contribute less than 0.3%. The same is true for the contribution of R_L , hence, the value of these resistors is not critical for the CNR of the ring oscillator with stacked active inductances.

IV. EXPERIMENTAL RESULTS

The ring oscillator with stacked active inductances and buffered outputs has been realized in the specified BiCMOS process [8]. The micrograph of the IC is shown in Fig. 5. The active chip area of the oscillator with V/I converter is less than 0.13 mm^2 . Total chip area including bond pads is $1.5 \text{ mm}^2 \times 1.5 \text{ mm}^2$. The power dissipation of the total IC is 230 mW, of which 75 mW is dissipated by the VCO core. The power supply voltage is 2.7 V. All measurements have been performed on packaged samples (16 pins HTSSOP package). On-chip 50- Ω I/Q buffers provided the quadrature output signals with -20 -dBm output power.

Measured frequency and CNR versus differential tuning voltage V_{tune} are shown in Fig. 6. The tuning range is 16% and

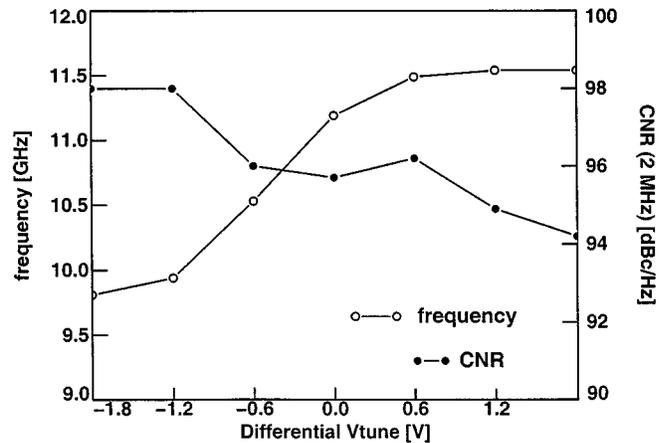
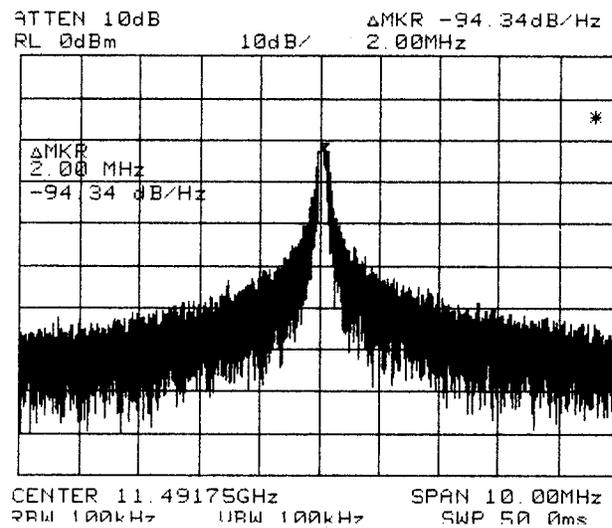
Fig. 6. Frequency and CNR (2 MHz) versus differential tuning voltage V_{tune} .

Fig. 7. Power spectrum of the oscillator at 11.5 GHz.

ranges from 9.8 to 11.5 GHz. The CNR was measured with a spectrum analyzer and results were verified with HP3048 phase noise measurement equipment which has an accuracy of ± 2 dB. Measured CNR at 2-MHz offset is better than 94 dBc/Hz over the complete tuning range. Best case CNR (2 MHz) is 98 dBc/Hz at 9.8 and 10 GHz. At higher frequencies, the carrier is somewhat smaller, resulting in a worst case CNR (2 MHz) of 94 dBc/Hz. The power spectrum of the ring oscillator at an oscillation frequency of 11.5 GHz is shown in Fig. 7, with a resolution bandwidth of 100 kHz.

V. BENCHMARKING

Ring oscillators reported in the literature are realized in a variety of IC technologies, ranging from CMOS, BiCMOS, and SiGe to InP and GaAs implementations. A number of reported ring oscillators are compared with the presented quadrature

TABLE III
RING OSCILLATOR BENCHMARKING

Ref.	CNR [dBc/Hz]	f_m MHz	f_{osc} GHz	P_{DC} mW	I/Q	Process/ f_T - / GHz	f_{osc}/f_T	CNR _{norm} [dBc/Hz]
This Work	94.3	2	11.5	75	Yes	BiCMOS/30	0.38	150.4
[10]	97	1	10	250	No	InP HBT/ 53	0.19	153
[11]	–	–	6.5	–	Yes	AlGaAs, GaAs/ 22	0.3	–
[2]	100	10	9	850	Yes	Si Bipo./ 25	0.36	130
[12]	75	1	2.2	1.3	No	BiCMOS/ 18	0.13	140.7
[13]	114	10	10	–	Yes	SiGe/ 45	0.23	–
[14]	94	1	2.2	11.8	No	0.5 μ m CMOS/ \sim 15	\sim 0.15	150.2
[5]	98.5	1	5.43	40	Yes	0.25 μ m CMOS/ \sim 40	\sim 0.14	157.2
[15]	82	0.1	1.8	22.5	Yes	Bipolar/ 18	0.1	153.5
[6]	106	2	2.2	100	Yes	BiCMOS/ 11	0.2	146.8

oscillator design. This comparison is shown in Table III. The figure of merit CNR_{norm} in Table III is defined as [8]

$$CNR_{norm} = CNR - 10 \log \left[\left(\frac{f_m}{f_{osc}} \right)^2 \frac{P_{total}}{1 \text{ mW}} \right] \quad (1)$$

and assumes a 6-dB-per-octave phase noise slope versus offset frequency f_m . Parameter P_{total} is the total power dissipation of the oscillator (excluding buffers).

The realized quadrature oscillator achieves a state-of-the-art f_{osc}/f_T ratio in comparison with the other listed ring oscillators. The ring oscillator in [2] with f_{osc}/f_T equal to 0.36 comes close to the achieved record of 0.38, but has a normalized CNR which is 20 dB lower compared to the ring oscillator circuit with stacked active inductances.

VI. CONCLUSION

In this paper, a two-stage ring oscillator with stacked active inductances has been presented. The oscillator can be tuned between 9.8–11.5 GHz and is suitable for use in DCR circuits of optical receivers which require quadrature signals. The active inductances isolate the oscillator core from cascaded circuits, which makes the circuit relatively insensitive to loading effects. The quadrature oscillator is realized in a 30-GHz f_T BiCMOS technology and achieves an oscillation frequency over f_T ratio of 0.38. The CNR at 2-MHz offset is 94 dBc/Hz or better, which is realized with 75-mW dissipation and a 2.7-V supply voltage.

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