

# A Low-Phase-Noise Reference Oscillator with Integrated pMOS Varactors for Digital Satellite Receivers

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**Abstract**—A low-phase-noise LC reference oscillator (RO) for use in digital satellite receivers is described. This RO is an essential building block of a double-loop wide-band tuning system that reduces the phase noise of integrated quadrature voltage-controlled oscillators (VCO's) required for zero-IF receivers. In order to achieve a high degree of integration the RO is implemented using integrated varactors. Three varactor options which are available in a standard 11-GHz  $f_t$  bipolar technology are investigated: the p-n-junction of an NPN, an active varactor circuit, and a pMOS varactor. Experimental results show that the integrated pMOS varactor combined with external inductors is the preferred choice to implement the resonator of the low-phase-noise RO. The achieved tuning range is 225–310 MHz. Carrier-to-noise levels of more than 87 dBc/Hz at 10-kHz offset are measured. The performance is realized with a RO dissipation of 14 mW at a supply voltage of 3.5 V.

**Index Terms**—bipolar transistor oscillators, phase noise, satellite communication, varactors, VHF oscillators.

## I. INTRODUCTION

CONSUMER market developments, especially cost and size reduction, have resulted in digital satellite receivers utilizing zero-IF architectures [1]–[3]. This architecture allows a very high degree of integration. In this concept, the local oscillator (LO) in the tuning system is tuned to a wanted input satellite channel and this channel is directly downconverted to baseband. Although the zero-IF architecture allows almost full integration, it also demands additional complexity of the tuning system compared to a superheterodyne receiver. Zero-IF receivers require quadrature (I/Q) LO signals covering the total input frequency range [4]. In addition, the LO and the tuning system should be constructed in such a way that LO self-reception [5], which is caused by LO leakage [4] to the antenna, is minimized.

A fundamental solution to above mentioned problems is the double-loop architecture shown in Fig. 1 [6], [7]. In this architecture a fully integrated RC oscillator provides the needed I/Q signals in the satellite frequency band [8]. The phase-noise level of this oscillator is typically 20 dB higher than the noise level required for QPSK reception. Therefore, the RC oscillator is wide-band locked (1–2 MHz) to a low-noise tunable reference oscillator (RO) as shown in Fig. 1. The RO oscillates at a much lower frequency than the wanted satellite channel and cannot cause or contribute to pulling or self-reception problems.

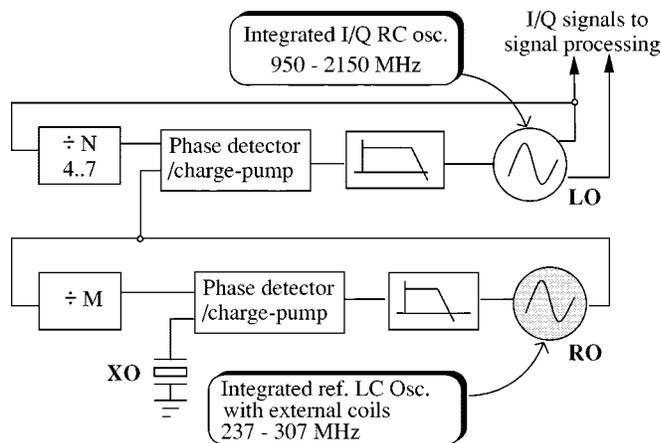


Fig. 1. Double-loop tuning system for digital satellite receiver front ends.

In order to select a satellite channel, the RO is part of a second phase-locked loop (PLL) and locked to a crystal oscillator reference (XO). Typical bandwidth of this second loop is 10 kHz.

In the presented architecture, the main divider  $N$  (Fig. 1) is programmable in four steps from 4 to 7. The integrated RC oscillator has four frequency bands, each successive band corresponding to a successive division ratio [6]. The advantage of having  $x$  bands is a reduction of the needed tuning range of the RO with roughly a factor  $x$ . In practice this reduction factor is somewhat smaller than  $x$ , because the bands need some overlap. Furthermore, the gain constant (in megahertz per volt) of the RC oscillator is reduced by the same factor, making it more robust against on-chip disturbances. The consumer satellite band starts at 950 MHz and extends to 2150 MHz. With four LO frequency bands the minimum tuning range of the RO is 237.5 MHz (950 MHz/4) to 307.2 MHz (2150 MHz/7).

One possible implementation of the RO is an off-the-shelf VHF oscillator with a completely external resonator circuit. However, in order to comply with the low-cost demands of the consumer market, a higher degree of integration is desirable. In this paper the options for varactor integration in a standard 11-GHz  $f_t$  bipolar process are investigated leaving the inductor off-chip. In this IC technology also a pMOS device is available which is generally used for switches and high-ohmic inputs. Experimental results will show that this pMOS—when used as a varactor—out-performs p-n-junctions and active variable-capacitance circuit topologies in the RO circuit of the double-loop tuning system.

## II. REFERENCE OSCILLATOR SPECIFICATION

The challenge of the RO design is meeting both carrier-to-noise ratio (CNR) and tuning range requirements. Next to CNR

Manuscript received December 20, 1999; revised March 16, 2000.

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Publisher Item Identifier S 0018-9200(00)06455-6.

and tuning range, power dissipation is the third important functional specification which follows from the system specification. The dc current of the RO must be limited to a few milliamperes in order to fit into the total power budget (500 mW) of the satellite front end. In order to derive the specification of the RO's resonator, the CNR and tuning requirements will be translated into resonator specification. This will be done using first-order equations modeling CNR and tuning range which establishes a lower limit for the resonator specification.

For digital satellite QPSK reception, the jitter specification is  $2.8^\circ$  RMS [9]. This translates to CNR requirements for the RO ranging from 85 to 95 dBc/Hz at 10 kHz offset of the carrier, depending on the integrated RC oscillator phase-noise level and symbol rate of the satellite system [6]. These low-phase-noise levels imply a minimum quality factor ( $Q_{\text{var}}$ ) for the integrated varactor of the RO.

For an LC oscillator modeled with an ideal transconductance amplifier (noise figure  $F = 0$  dB) and parallel LC circuit, the CNR is related to the carrier current, the loaded  $Q$ , the inductance, and the oscillator frequency as follows:

$$\text{CNR}(f_m) = -10 \log \left( \frac{FkT}{4\pi Q_l^3 I_{\text{rms}}^2 L} \frac{f_{\text{osc}}}{f_m^2} \right) \quad (1)$$

where

- $Q_l$  loaded  $Q$  of the parallel resonator;
- $k$  Boltzman's constant ( $1.3810^{-23}$  J/K);
- $T$  absolute temperature (300 K);
- $I_{\text{rms}}$  carrier current (0.5 mA rms);
- $f_m$  offset frequency (10 kHz);
- $f_{\text{osc}}$  oscillation frequency (307 MHz);
- $L$  resonator inductance value (30 nH).

Solving (1) for  $\text{CNR}(10 \text{ kHz}) = 90 \text{ dBc/Hz}$  and with the values of the (design)-parameters, the minimum loaded quality factor  $Q_l$  of the RO resonator calculates to 5. Since in practice the active RO part has  $F > 0$  dB and the needed dc current to realize  $I_{\text{rms}}$  at the fundamental frequency is much larger than  $I_{\text{rms}}$ , the **unloaded** quality of the varactor  $Q_{\text{var}}$  should be significantly larger than 5. Therefore, if the inductor and the varactor of the RO oscillator have the same  $Q$ , the  $Q$  of each should be significantly larger than 10. This rules out the use of integrated coils in the IC technology in which the RO needs to be realized, because around 300 MHz the inductor  $Q$  will be less than 10. A cost-effective solution is an off-chip inductor, for example, an air coil or printed PCB coil. Both air coils and printed PCB coils can be realized with  $Q$ 's of 60 and better at 300 MHz. Hence the  $Q$  of the varactor is expected to dominate the  $Q_l$  value of the RO resonator. The conclusion is that  $Q_{\text{var}}$  must be significantly larger than 5 to meet the RO CNR specification.

Using the tuning range requirements for a four-band double-loop tuning system, the needed ratio ( $R_{\text{var}}$ ) of the maximum capacitance  $C_{\text{max}}$  to the minimum capacitance  $C_{\text{min}}$  can be calculated as follows:

$$R_{\text{var}} = \frac{C_{\text{max}}}{C_{\text{min}}} = \left( \frac{f_{\text{max}}}{f_{\text{min}}} \right)^2 + \frac{C_{\text{par}}}{C_{\text{min}}} \left( \left( \frac{f_{\text{max}}}{f_{\text{min}}} \right)^2 - 1 \right). \quad (2)$$

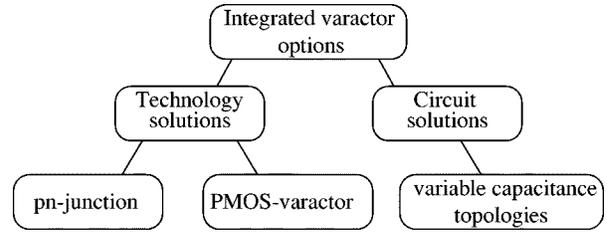


Fig. 2. Integrated varactor options.

In (2)  $f_{\text{max}}$  and  $f_{\text{min}}$  are the maximum and minimum RO frequency, respectively.  $C_{\text{par}}$  is the total fixed capacitance. Main contributors to  $C_{\text{par}}$  are the active oscillator circuit and interconnect parasitics. In the theoretical case that  $C_{\text{par}}$  equals zero, the minimum varactor ratio  $(307.2/237.5)^2$  calculates to 1.67. In Section IV the active oscillator circuit will be described and this circuit will contribute 3.8 pF at 307 MHz to  $C_{\text{par}}$ . Recalculation of (2) with this value of  $C_{\text{par}}$  and substituting for  $C_{\text{min}}$  5.2 pF (which follows from  $L = 30$  nH and 307 MHz), results in a minimum  $R_{\text{var}}$  of 2.16. The derived minimum varactor  $Q$  (of 5)  $Q_{\text{var}}$  and minimum capacitance ratio  $R_{\text{var}}$  (of 2.16) can now be used to benchmark the available varactor options in a standard IC technology.

### III. VARACTOR OPTIONS

In the bipolar IC technology used for the RO design, three varactor options are available. The three alternatives are presented in Fig. 2. Passive options are the p-n-junction varactor and the pMOS varactor. Using active devices, circuit solutions can be realized which implement a variable capacitance.

#### A. The p-n-Junction Varactor

In a bipolar process<sup>1</sup> a p-n-junction type varactor is readily available, for example, by connecting the emitter to the base of a transistor and using the collector-base junction reverse biased. Alternatively the base-emitter junction can be used. Generally, the collector-base junction has a higher breakdown voltage ( $BV_{\text{bco}}$ ) than the base-emitter junction breakdown voltage ( $BV_{\text{beo}}$ ). In the available IC technology  $BV_{\text{beo}}$  is 4.5 V and  $BV_{\text{bco}}$  is 6.5 V so the collector-base junction is a more robust choice.

Fig. 3 shows the simulated capacitance curve of 20 NPN's in parallel with base and emitter short-circuited. Each transistor has an emitter area of  $1.6 \mu\text{m} \times 200 \mu\text{m}$ . The zero reverse voltage bias capacitance of this p-n-junction type varactor is 12.4 pF. Simulated capacitance is mainly the sum of collector-base junction capacitance  $C_{\text{cb}}$  and collector-substrate junction capacitance  $C_{\text{cs}}$ . The junction grading coefficients of these junctions are 0.25 and 0.42, respectively. The simulated capacitance ratio is 1.9 with reverse-bias voltage  $V_{\text{tune}}$  varying from 0 to 5 V. However, since the RO will be incorporated in the double-loop tuning system, zero reverse voltage is unrealistic, since voltage head room is needed for the charge-pump in the tuning system. Furthermore, the oscillator voltage swing will limit the usable tuning range. The capacitance ratio with 0.5–5-V reverse bias

<sup>1</sup>In a standard CMOS process available parasitic p-n-junctions could be used [10], although they are generally not well characterized.

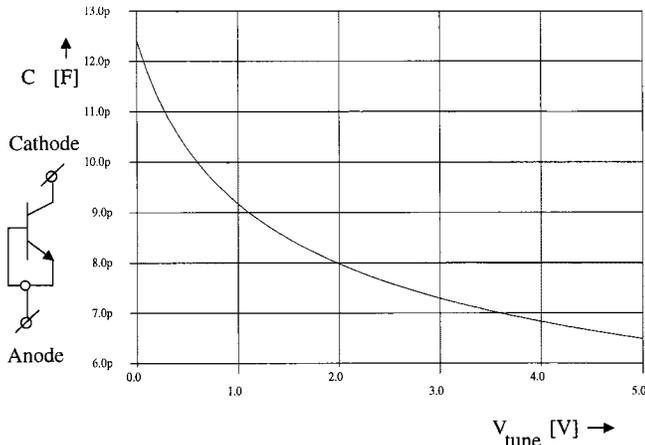


Fig. 3. Capacitance curve of the p-n-junction varactor.

is for example reduced to 1.6 which is less than the minimum  $R_{\text{var}}$ .

Unloaded  $Q$ 's of p-n-junctions are measured in the range of 75 and higher at 1 GHz [11]. Therefore varactor  $Q$ 's in excess of 75 can be expected at 300 MHz, and phase-noise performance is expected to meet the requirements of 85 dBc/Hz at 10 kHz-offset of the carrier.

### B. Variable Capacitance Topologies

Circuit topologies can be used to emulate a varactor function. Large tuning ranges can be achieved at high frequencies using variable impedance converters [12]. When using variable capacitance topologies to implement a varactor function, simulations indicate that large  $C_{\text{max}}/C_{\text{min}}$  ratios can be accomplished. However it is expected that the additional noise of the active devices degrade the spectral purity of the oscillator severely compared to passive tuning solutions.

In order to investigate the properties of a variable capacitance solution an architecture based on current multiplication is explored. The concept and transistor implementation are shown in Fig. 4(a) and (b), respectively. From the behavioral model in figure Fig. 4(a), (3) can be derived.

$$\frac{V_x}{I_x} = \frac{1}{j\omega \left( \frac{C}{2}(1 + \alpha) \right)}. \quad (3)$$

In (3)  $C$  is the fixed capacitance and  $\alpha$  the variable current multiplication factor. The concept is realized using a Gilbert cell to implement the current multiplier [Fig. 4(b)]. The simulated capacitance curve of the variable capacitance topology is shown in Fig. 5 (solid curve). Simulated  $C_{\text{max}}/C_{\text{min}}$  ratio (5.3 pF/0.7 pF) is 7.6. Note that the tuning curve can be linearized by driving the current multiplier tuning voltage via two diode-connected transistors [13]. Fig. 5 (dashed curve) shows the equivalent input noise current density  $I_{\text{noise}}$  of the active varactor versus tuning voltage  $V_{\text{tune}}$ . When the Gilbert cell is in balance ( $\alpha = 0$ ),  $I_{\text{noise}}$  reaches its maximum of 24 pA/ $\sqrt{\text{Hz}}$ . The varactor capacitance is 3 pF at this point. In order to be able to compare this varactor

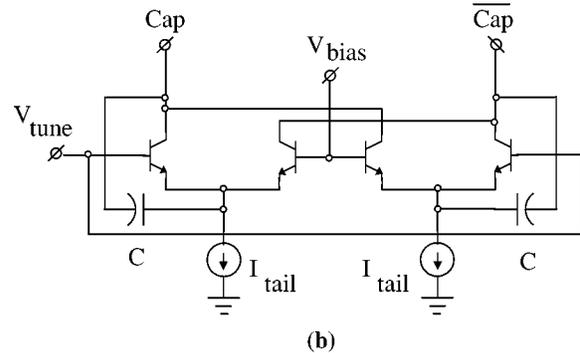
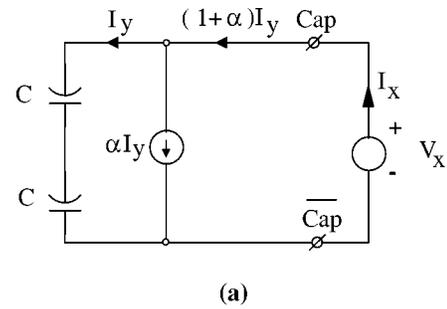


Fig. 4. Variable capacitance topology. (a) Behavioral model. (b) Implementation with a Gilbert cell.

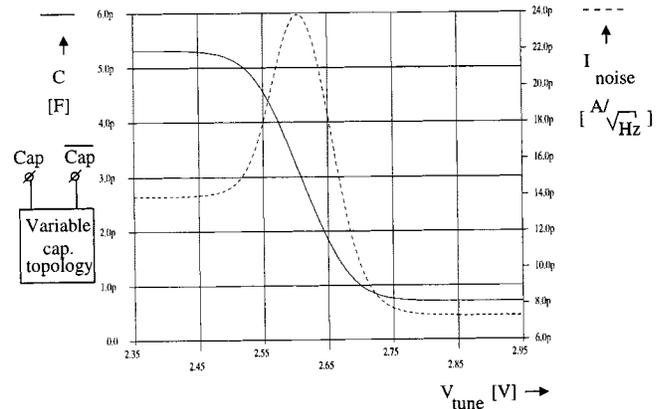


Fig. 5. Capacitance curve of the active varactor and its equivalent input noise current density versus  $V_{\text{tune}}$ .

with the  $Q$  specification, it is needed to define an equivalent quality factor  $Q_{\text{equivalent}}$ , as follows.

$$Q_{\text{equivalent}} = Q_{\text{var}} \frac{I_{nr}}{I_{ntot}} \quad (4)$$

where

$Q_{\text{var}}$  varactor  $Q$  ( $2\pi f_{\text{osc}} C_{\text{var}} R_p$ );

$I_{nr}$  noise current density of resistor  $R_p$  ( $\sqrt{4kT/R_p}$  A/ $\sqrt{\text{Hz}}$ );

$I_{ntot}$  total equivalent noise current density of active varactor (A/ $\sqrt{\text{Hz}}$ ).

$Q_{\text{var}}$  is the standard definition of the  $Q$  at oscillation frequency  $f_{\text{osc}}$  of a capacitance (here  $C_{\text{var}}$ ) connected in parallel with a resistor (here  $R_p$ ) which models its noise and losses. For an active varactor this  $Q$  definition is too optimistic since it does

not take into account the noise of the active devices in the varactor.  $Q_{\text{equivalent}}$  includes the additional noise sources of the active devices and can be directly used in (1) for CNR calculations. When  $I_{n\text{tot}}$  reaches its maximum of  $24 \text{ pA}/\sqrt{\text{Hz}}$ ,  $R_p$  is  $1 \text{ k}\Omega$  at  $307 \text{ MHz}$  and  $C_{\text{var}}$  is  $3 \text{ pF}$  (simulated).  $Q_{\text{var}}$  calculates to  $5.8$  and  $Q_{\text{equivalent}}$  becomes  $1$ . Therefore, especially in the middle of the tuning range, a poor CNR can be expected and RO CNR specification will not be met.

### C. The pMOS Varactor

In case of a CMOS implementation of the RO both nMOS and pMOS devices can be used to implement a MOS-type varactor. Due to higher carrier mobility, nMOS-type varactors will yield higher  $Q$ 's. For MOS-type varactors  $C_{\text{max}}/C_{\text{min}}$  ratios of more than 3 have been demonstrated and  $Q$ 's larger than 20 at  $1 \text{ GHz}$  have been measured [14]. However, the required RO phase-noise levels have not been demonstrated yet. In the technology available for the RO design, only pMOS devices were present. Based on device physics of the two-terminal MOS structure [15], the tuning physics of the oscillator under design can be predicted. Fig. 6 shows the dependence of the pMOS bulk-gate capacitance  $C_{\text{bg}}$  on the bulk-gate voltage  $V_{\text{bg}}$ . In "strong" accumulation and strong inversion  $C_{\text{bg}}$  becomes eventually equal to  $C_{\text{ox}}$  which is the oxide permittivity over oxide thickness per unit area. In between these extremes,  $C_{\text{ox}}$  is connected in series with a capacitance which depends on the type and number of carriers under the gate oxide and  $C_{\text{bg}}$  will change substantially. Fig. 7 shows the simulated capacitance curve of the pMOS varactor. The simulated device has a  $W/L$  of  $200 \mu\text{m}/1.2 \mu\text{m}$  and is built up with 20 devices in parallel. Hence the total width of the varactor is  $4000 \mu\text{m}$ . The bulk (or more accurately the n-well) is connected to the drain and source contact and forms the varactor cathode. The gate terminal acts as anode. MOS-model level 9 [16] is applied for the modeling of the device characteristics. In the simulation, the anode was given a fixed reference voltage of  $2.5 \text{ V}$  to be able to evaluate the accumulation region and inversion region with positive tuning voltages. Simulations show a minimum and maximum capacitance of  $3.6$  and  $11.3 \text{ pF}$ , respectively. This results in a  $C_{\text{max}}/C_{\text{min}}$  ratio of  $3.1$ . In the applied MOS model, source, drain, and channel resistance are not modeled which results in unrealistic  $Q$  predictions. The  $Q$  of the pMOS varactor will be evaluated in a RO design.

Table I summarizes the evaluation of the varactor options. The quality of the varactor and the capacitance ratios are compared with the varactor specifications derived in Section II. The pMOS-type varactor is the only option for the RO design with integrated varactors, but its  $Q$  is an uncertainty. The simulation results and expectation of the pMOS varactor will be experimentally verified. To enable characterization of the pMOS varactor, a robust active oscillator circuit is needed. In the following section, the design of this active circuit will be discussed, followed by a presentation of the experimental results in Section V.

## IV. REFERENCE OSCILLATOR DESIGN

In Fig. 8 a simplified diagram of the RO is presented. A fully balanced design is chosen in order to minimize interference via supply lines in a mixed-signal satellite receiver IC. The design consists of a cross-coupled pair which implements the needed

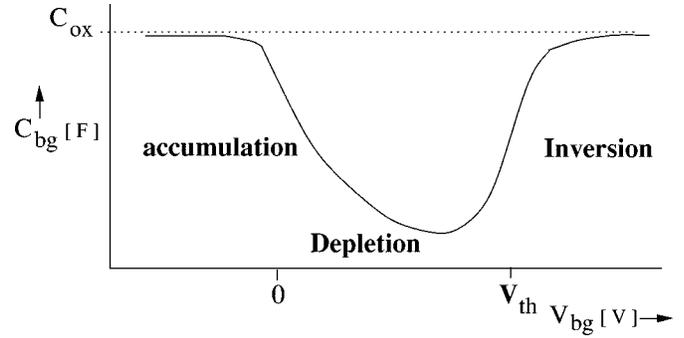


Fig. 6. PMOS capacitance regions versus  $V_{\text{tune}}$ .

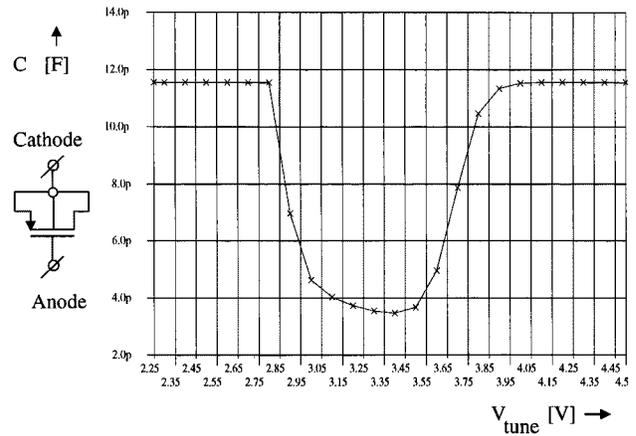


Fig. 7. Simulated capacitance curve of the pMOS-junction varactor.

TABLE I  
BENCHMARKING OF THE VARACTOR OPTIONS

Varactor-option	$Q_{\text{var}}$	$R_{\text{var}}$	Conclusion: usable?
	Spec: $> 5$	Spec: $> 2.16$	
PN-junction	$> 75$	$< 1.9$	no
Active varactor	1	7.6	no
PMOS	?	3.1	possibly

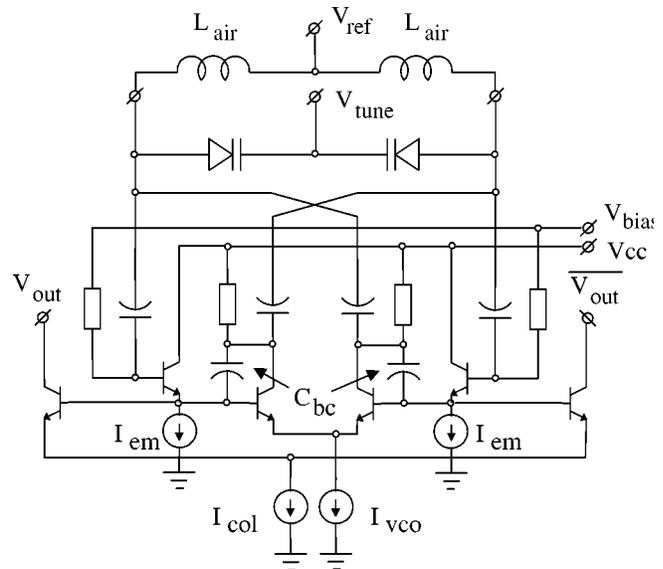


Fig. 8. Reference oscillator circuit diagram.

negative transconductance. The tank is connected to the differential pair via two emitter followers. The open-collector differential pair facilitates measurements and the collectors can be directly connected to  $50\ \Omega$  measurement equipment. Power dissipation of the cross-coupled pair and the emitter followers [the voltage-controlled oscillator (VCO) core] is 14 mW. During the design, simulations revealed potential parasitic oscillations in the frequency range of 1.5 to 2.5 GHz caused by package and PCB parasitics. To eliminate these oscillations which would obstruct proper characterization, base-collector ( $C_{bc}$  in Fig. 8) capacitances are added. This reduces oscillator activity at high frequencies.

The tank circuit is capacitively coupled to the active RO part by high  $Q$  ( $>100$  at 300 MHz) on-chip capacitors. In this RO design, air coils are used having  $Q$ 's better than 100 at 300 MHz. The capacitance curve of the pMOS varactor versus  $V_{tune}$  can be mapped to the wanted dc range with  $V_{ref}$ .  $V_{ref}$  effectively is changing the threshold voltage  $V_{th}$  of the pMOS varactor. For  $V_{ref}$  equal to zero, part of the tuning range in the accumulation area has negative  $V_{tune}$ . By making  $V_{ref}$  equal to, for example, 2.5 V, the complete tuning range can be covered with positive tuning voltages (as shown in Fig. 7).

## V. EXPERIMENTAL RESULTS

The RO test IC with pMOS varactor has been realized with a 5-V voltage stabilizer which generates the 3.5-V supply voltage  $V_{cc}$  and the 2.7-V bias voltage  $V_{bias}$ . The chip micrograph of the RO with pMOS varactors is shown in Fig. 9. Active IC area is  $0.26\ \text{mm}^2$ . An eight-pins plastic shrink small outline (SSO) package is used for packaging.

Simulated and measured oscillation frequency versus  $V_{tune}$  are shown in Fig. 10. As can be expected from the MOS capacitance behavior (Fig. 6), the frequency curve is not monotone. The frequency curve in the inversion region is well predicted by the applied MOS model, but the modeling needs improvement to predict the accumulation region accurately. The minimum and maximum frequency of the RO are 225 and 310 MHz, respectively. The complete tuning range needed for the RO is covered and more than 31% tuning range is measured.

Measured phase noise at 10-kHz offset of the carrier over the complete tuning range is presented in Fig. 11. Over the entire RO tuning range the CNR is better than 87 dBc/Hz at 10 kHz and specification is met.

## VI. DISCUSSION

Characterization of the RO design with integrated pMOS varactors shows that the pMOS solution meets both phase noise requirements and tuning range requirements. However, for a robust product, additional effort is needed. Measurements have been performed with air coils and these should be replaced by printed PCB coils for two reasons. First, this will remove an alignment point since the PCB coils are much more reproducible than air coils. Second, air coils are susceptible to microphonics which can lead to cycle slips in the satellite receivers. In order to cope with process spread more tuning range is needed. This can be achieved by a redesign of the active RO circuitry and optimizing for minimum  $C_{ro}$ . Furthermore, if the minimum varactor

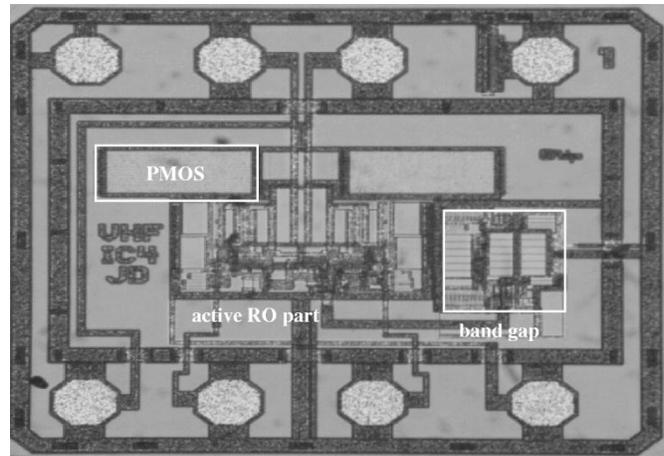


Fig. 9. Die photo of the RO with pMOS varactors.

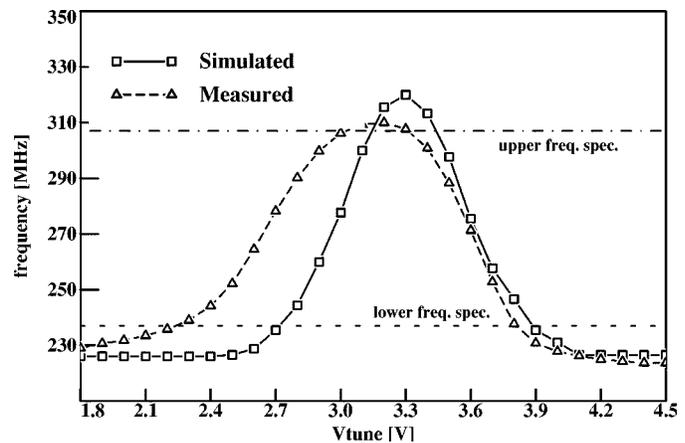


Fig. 10. Frequency versus  $V_{tune}$ .

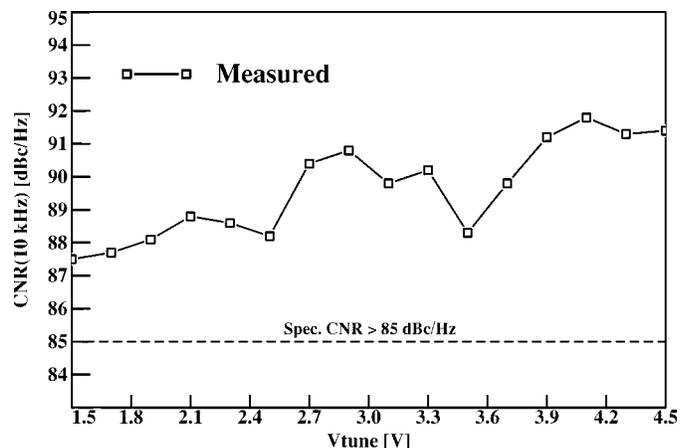


Fig. 11. CNR(10 kHz) versus  $V_{tune}$ .

capacitance  $C_{min}$  is increased, the (relative) influence of  $C_{par}$  [see (2)] reduces and the tuning range increases.

The tuning behavior of the RO with pMOS varactors is not monotone. In the test IC, the well of the pMOS is connected to the drain and source contact. This allowed evaluation of both accumulation region and inversion region of the varactor. Since the RO will be part of the double-loop tuning system, the tuning curve needs to be made monotone otherwise the double-loop

tuning system could latch up. This can be realized by connecting the well-contact to  $V_{cc}$ . Depending on whether the gate is connected as anode or as cathode the accumulation region or inversion region can be selected for operation. Fig. 10 shows that the accumulation region (left region) has a lower VCO gain (MHz/V) which leads to lower spurious components resulting from noise sources present at the tuning input.

The  $Q$  of the pMOS varactor can be improved by careful optimization of the layout. In the presented design, standard layout rules are applied. Using the design guidelines in [14] the layout of the pMOS varactor can be optimized to maximize the  $Q$  and thus the phase-noise performance of the RO.

## VII. CONCLUSIONS

For the first time pMOS integrated varactors are successfully used to realize an RO for a double-loop tuning system, which can be used in digital satellite receiver architectures. State-of-the-art phase-noise performance of 87 dBc/Hz at 10-kHz offset is experimentally demonstrated for a wide-band oscillator having integrated varactors. Measured tuning range is 225 to 310 MHz, which is larger than 31%.

## ACKNOWLEDGMENT

The authors would like to thank M. Tavares for her help during realization of the oscillator. Also, discussions with L. de Maaijer concerning MOS modeling and performance contributed significantly.

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