HW/SW Co-design for SoC on Mobile Platforms

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Abstract

Portable platforms like cell phones, PDA's, and notebooks get more and more feature-packed every year. Given the very short life-cycles of these products, the set-maker has to be able to add additional selling-features like for example FM/AM radio, TV, and wireless links with a minimum of risk, board space, minimum power consumption and cost onto it's already existing product platform. Systems on Chip (SoC) in their truest sense, having no external components, and that are optimized for flexibility and low power consumption are the solution to this challenge. This paper discusses the key features and key circuits of the first "no-external components" FM radio and TV tuners for mobile platforms. Both SoCs make use of resources that are generally available on mobile platforms like a reference clock and a microprocessor. The signal processing path of both ICs is fully controlled by software and adaptable as a result of hardware/software co-design. For the set-maker, both ICs can be virtually treated as digital ICs as there are no "hot" RF components off-chip, nor is any other component off-chip. RF building blocks like a broadband tunable LNA (on the TV IC) and a I/Q oscillator (on the FM IC and TV IC) are discussed in detail.

1 Introduction

Mobile phones are these days packed with features, such that the name mobile phone only refers to one of many possible functions of the portable device. Radio, MP3 player functionality, games, PDA functionality (smart phones) are already a commodity, and soon analog and especially digital TV (e.g. DVB-H) will be accepted as standard features on a mobile phone [1, 2, 3, 4].

All these "add-ons" with respect to the primary function of being able to make phone calls and receive them, have similar constraints. Obviously they should be cheap (minimum bill of material and IC die size), the volume a function needs should be minimum, and the power consumption should be a low as possible as the application should not drain the battery of the phone too fast, making it's primary function questionable. Apart from the mentioned constraints/challenges one could summarize other requirements as "anything that might be of importance getting a design-win into as much portable platforms as possible". This "anything" certainly includes having a minimum of "hot" RF signal nodes outside the chip or package. Each RF spot outside the chip or package complicates board design for a set-maker, requires specialistic RF expertise and is a potential source of EMC problems.

In general, two approaches are followed to cope with the described challenges and the everlasting pressure to reduce cost of features like MP3 functionality, radio and TV. The first is the (full) System-on-a-Chip (SoC) approach and the second is the System-in-a-Package (SiP) approach. SiP can be very attractive as technologies can be mixed and high-Q substrates can be combined with silicon dies and external passive components. This can result in cost-effective solutions with state-of-the-art performance while the set-maker only has to deal with one component. SoC, on the other hand, does not require the built-up and investment of complicated packaging solutions and, since it has to deal with less interfaces between dies and external components can be more cost and power efficient.

For a successful SoC approach, analog and digital partitioning as well as the optimum division between hardware and software is of prime importance. This paper discusses two examples where, a complete radio and multi-standard TV receiver are integrated on one silicon die, without the use of any external component. This is achieved by making optimum use of the resources already available on portable platforms (such as a micro-processor and a reference clock), by designing the high-performance signal path in the analog domain, and having full software control over these signal processing blocks by digital control logic. In section 2 the FM radio is highlighted and two of of its key building

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blocks: the linear demodulator and the wide range I/Q oscillator, are analyzed. In Section 3, the architecture of the monolithic multi-standard TV receiver is discussed together with a more in depth study of its LNA and the quadrature RF oscillator.

2 No external components FM radio

2.1 Architecture

On mobile platforms such as phones, a micro-processor, a reference oscillator, and user interfaces are readily available. These resources are also used in the case of the FM radio architecture shown in Fig. 1 [5]. A low-IF architecture is chosen like in [6]. After down-conversion of the desired channel, fully integrated selectivity has been implemented. The improved selectivity filters are temperature compensated and digitally programmable. In this way the micro-controller can correct not only the spread in the process parameters, but also can perform circumstantial control functions like reduction of the bandwidth [6] in poor reception conditions. The adjustment of all characteristic frequencies of filters and oscillators will be performed by the micro controller. Due to the use of frequency locked loops (FLLs) instead of Phase locked loops (PLL) the frequency of the crystal can be freely chosen to achieve minimum overall cost. For the control of the RF oscillator a capacitance bank is used to improve the ripple rejection and to avoid a large and noise sensitive tuning voltage [7]. The whole radio signal path is controlled by several AGC's to process all signals in a linear mode. This is to avoid intermodulation products, folding and repeat spot reception. The result is shown in the improved dynamic selectivity. The IF frequency is chosen at 110 kHz to allow 30% over-modulation. Due to this choice the image reception is positioned in the slope of the dynamic selectivity. The key elements that enabled zero external components for this "FM-radio SoC" are a high performance analog signal processing path with many dedicated novel IP blocks that are all software controlled, and re-use, where possible, of the platform resources.

2.2 Linear FM Demodulator and I/Q oscillator

The architecture of the PLL demodulator is shown in Fig. 2. The quadrature IF signals are fed into a linear demodulator for maximum sensitivity. Through software control (via the DAC) errors introduced by processing spread or temperature spread are minimized. The output of the demodulator is the MPX signal, which is fed into the stereo decoder (as shown in Fig. 1).

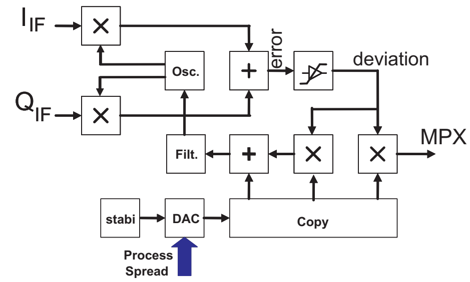

Figure 2. Block diagram of the linear FM demodulator.

The demodulator in Fig. 2 requires an oscillator with a tuning range of a factor of 300 (1 kHz to more than 300 kHz), and with a high linearity in the tuning curve to meet the 0.5 % THD requirement. Two-integrator oscillators can have a large linear tuning range, but latch-up danger limits the lower boundary of its tuning range [8].

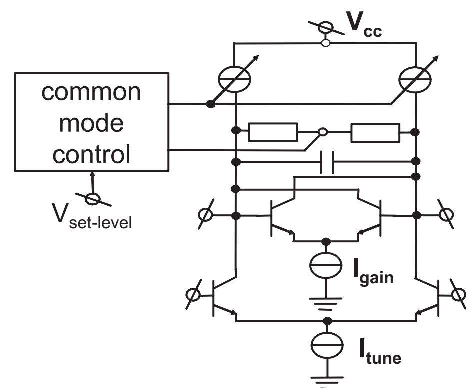

Figure 3. One section of the wide range I/Q oscillator.

In Fig. 3, one of the two stages of an improved two-integrator oscillator is shown [1]. In conventional two-integrator oscillators the controlled current sources in the collectors are simple collector resistors (R_c). The frequency of this oscillators is proportional to I_{tune}. When I_{tune} becomes smaller than current I_{gain}, which controls the output voltage level, the oscillator latches up. Current I_{gain} is inversely proportional to the mentioned collector resistors R_c. Increasing this resistor the lower tuning range limit can be extended. However, the voltage drop across R_c limits this option, especially at low supply voltages. This problem is solved in the enhanced circuit diagram of Fig. 3 where the

[1] Two of these stages plus an inversion form the total oscillator.

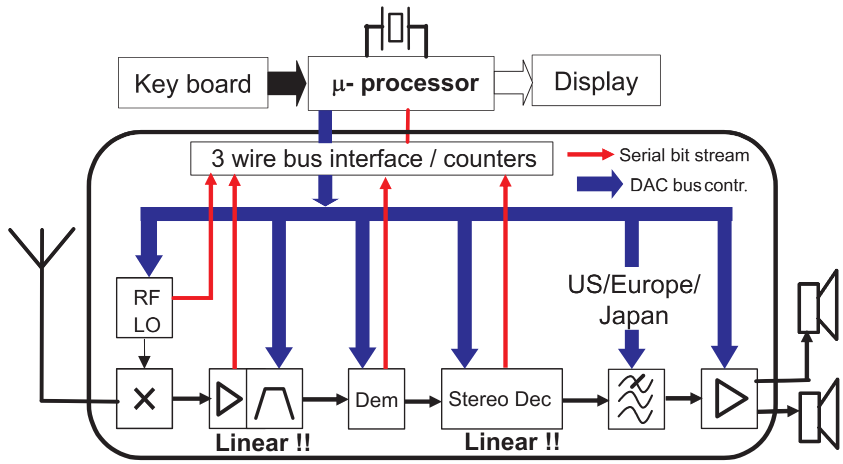

Figure 1. Block diagram of the no-external components FM radio.

DC current is provided by the controlled current sources. Now resistors have only an AC function. Therefore, the sense resistors can be made very large, I_{gain} very small, and the lower limit of the tuning range is lowered tremendously. To keep the transconductances of the oscillator in the linear range an AGC circuit is used.

2.3 Performance summary

A performance summary of the radio IC is given in Fig. 4.

Technology:	BICMOS 9 GHz f_T/ 0.6 μm
Chip area (mm²):	11
Power (mW):	46 (at 2.7 V)
Supply voltage (V):	2.7 - 7
Sensitivity (μV):	1
Image rejection (dB):	26
Stereo chan. sep. (dB):	30
THD (%):	0.7

Figure 4. FM radio specifications summary.

The FM radio IC is implemented in a 8 GHz f_T mainstream BiCMOS technology. Fig. 5 shows the chip micrograph. The total active chip area is 11 mm2. Its total power dissipation is 17 mA with a nominal supply voltage of 2.7. - 7 Volt.

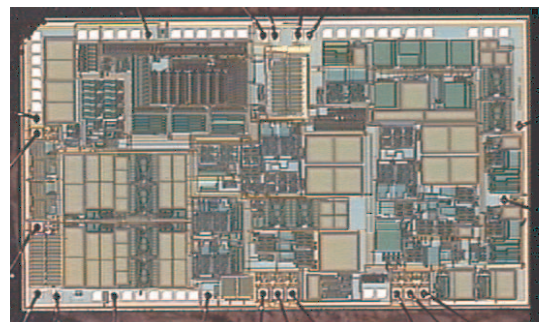

Figure 5. FM die photo.

3 No external components TV

3.1 Architecture

Fig. 6 (see next Page) highlights the architecture of the Universal Mobile TV (UMTV) chip. No front-end antenna filter is required because the LNA has built-in tunable selectivity (it's operation is described in the next section). After the LNA a system of mixers suppresses harmonics and a low-IF poly-phase filter follows. A feature of this fully integrated filter is that it can suppress the image up to 60 dB (Dynamica Image Suppression: DIS). Channel selectivity is followed by a split filter after which sound and video are demodulated. A low-IF quadrature output is provided for digital DVB-H demodulators. For the sound demodulator, the demodulator of the described FM radio could be fully re-used [5]. Identical to the FM radio, UMTV does not require external components. Also, every RF and IF building block is software controlled.

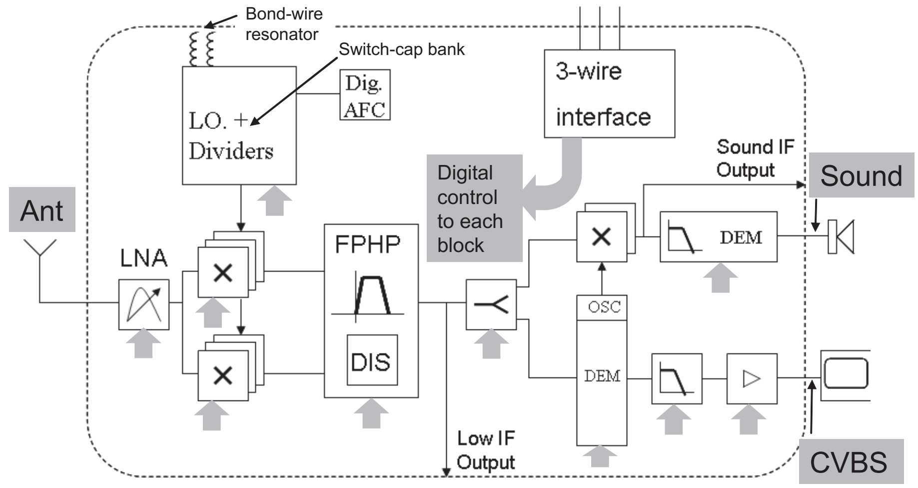

Figure 6. Block diagram of UMTV.

3.2 Low noise tunable amplifier

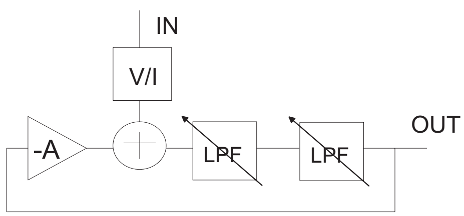

Figure 7. Broadband tunable amplifier.

The signal processing starts with a selective tunable Low Noise Amplifier (LNA). It plays a crucial role in obtaining the targets of high sensitivity and low power. The principle of the selective LNA is illustrated in the block-diagram in Fig. 7. The antenna signal is converted from voltage to current (V/I block). This current is injected in the loop of an inverter amplifier with gain -A and two low-pass filters (LPF). The cutoff frequency of the LPFs can be controlled with currents. The positive feedback with a phase shift of approximately 360° in the loop (180° due to the inverter and approximately 180° by the low pass filters) will tuned to different frequencies. By controlling the total gain in the loop, sufficient phase margin at gain > 1 is obtained to keep the loop stable. By making more phase shift in the loop (e.g. by adding more orders to the LPF), the quality factor will be higher and the shape of the curve will change. For an LNA to keep the noise at a low level, it is important to keep component count of the signal processing components as low as possible. This wideband tunable LNA concept can be designed in silicon with only 5 transistors and no dominant resistors in the signal path [9]. The selectivity curves of the LNA are given in Fig. 8. Frequency responses for various tuning currents are shown. The noise figure of the LNA plus mixers and IF filter (see Fig. 6) is always better than 9 dB over the total VHF and UHF band (40 MHz to 900 MHz) [9].

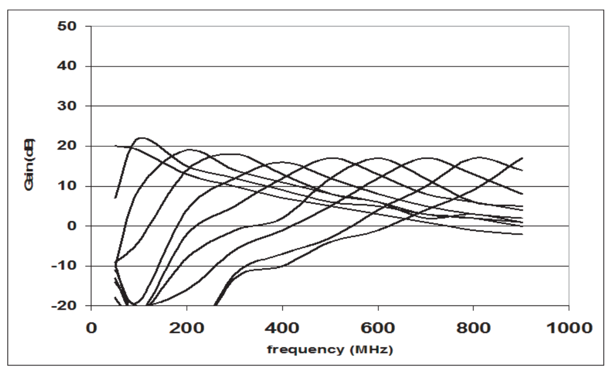

Figure 8. Measured selectivity curves.

3.3 Octave tunable oscillator

Another crucial subfunction of the UMTV chip is the LO. It is a quadrature oscillator circuit with integrated digital capacitance bank [5, 9] with a tuning range from 420 to 900 MHz. One section of the oscillator is shown in Fig. 9. The resonator in each section makes use of bond-wire inductors, which are together with the capacitor bank connected to i_{tank}. Unlike most I/Q oscillators no cross-coupled pair (thus eliminating a self-oscillation mode) is present within a section, making the circuit very robust against multi-mode oscillations, which are well-known in I/Q oscillators. Transistors Q7 and Q8 together with their external (and internal) base resistors implement active inductors that tune the total phase shift of each section close to 90°, thus realizing operation at the resonance frequency of the LC-tank circuit where the quality factor is maximum.

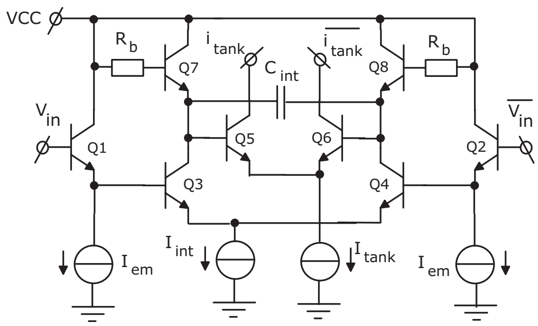

Figure 9. Octave tunable I/Q oscillator.

3.4 Performance summary

The UMTV IC is realized in a low-cost mainstream 8 GHz f_T BiCMOS process. The die photo (size 5*5 mm) of the complete multi-standard TV receiver is shown in Fig. 10. Total noise figure of the TV receiver is less than 9 dB and its 1 dB compression point is more than 80 dBμV.

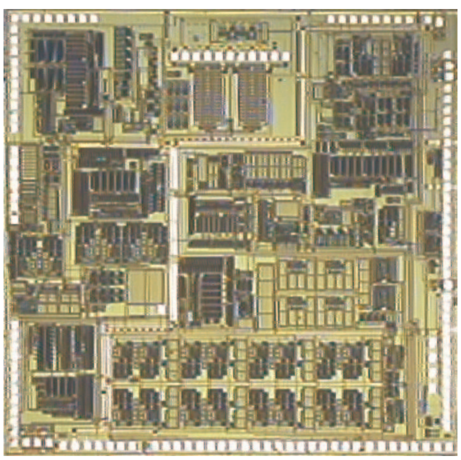

Figure 10. UMTV die photo.

4 Conclusions

Two innovative SoCs with no-external components are highlighted in this paper. The FM radio achieves a sensitivity of 1 μV and occupies only 11 mm^2. It incorporates a linear FM demodulator with a linear two-integrator oscillator that is tunable from 1 kHz to 300 kHz. The multi-standard TV receiver dissipates only 150 mW, covers all analog standards, and has a low-IF output for digital standards. Both ICs demonstrate how HW/SW co-design in low-cost BiCMOS processes, can eliminate all components, minimize required board space, while maintaining a high performance level for complex applications like complete FM radios and TV receivers on mobile platforms.

Acknowledgment

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