Explicit Design Equations for Class-E Power Amplifiers with Small DC-feed Inductance

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Abstract — **This paper presents novel, explicit design equations for Class-E power amplifiers with finite DC-feed inductance. A mathematically exact analysis of the idealized Class-E power amplifier with small DC-feed inductance shows that the circuit element values are transcendent functions of the input parameters. Therefore, the designer needs to perform a long iterative procedure in order to find these values. We have solved the circuit operation for a certain number of cases, and performed a Lagrange polynomial interpolation in order to obtain explicit, directly usable design equations. The proposed design method is verified by simulation and the agreement with the theory is excellent.**

1 INTRODUCTION

Since its introduction [1], the Class-E power amplifier (PA) has been a subject of significant interest in the research community. Many different aspects were thoroughly studied, and one of the most interesting of them is the Class-E operation without an RF choke. Using a finite DC-feed inductor instead of an RF choke (RFC) in the Class-E PA has a number of benefits. A small DC-feed inductor has lower loss due to a smaller electrical series resistance (ESR). Furthermore, the cost and the physical size of the circuit decrease, and the load resistance that has to be presented to the transistor increases, thus making the design of the matching network easier. Finally, using a small DC-feed inductance is important if the PA is to be used in an envelope elimination and restoration (EER) system [2]. Therefore, there is a strong interest to pursue the design of the Class-E PA with finite DC-feed inductance.

In [3], one of the first attempts was made to study this topic. Some other relevant papers include [4]-[5]. All these papers have in common that the procedure of obtaining final circuit elements is either long, complex and iterative [3][4], and does not provide a direct insight into the circuit design, or is too simplistic and not analytically exact [5]. Basically, the design of the Class-E PA with small DC-feed inductance is, from the mathematical point of view, a transcendent problem. Therefore, the designer needs to iteratively solve the system of equations for a certain set of input parameters, in order to obtain the final circuit element values. If any of the input parameters is changed, the calculation has to be repeated from the beginning. Thus, it is a tedious and highly impractical procedure.

In this paper we propose another approach to this problem. The system of transcendent equations is numerically solved for a certain number of discrete points of an input parameter, and the obtained results are interpolated by the Lagrange polynomial. The polynomial interpolation, if performed with a sufficient density of points on the segment of interest, provides adequate accuracy and can be used for any value of the input parameter on that segment. In other words, we obtain explicit, directly usable design equations for the Class-E PA.

The paper is organized as follows. In section 2, the principles of analysis of the Class-E operation with finite DC-feeder are described, and the numerical interpolation of the obtained results is shown. In section 3 a design example is given and the proposed design method is verified by simulation. The conclusion is drawn in section 4.

2 ANALYSIS AND INTERPOLATION

In this section we will study the operation of the Class-E PA with finite DC-feed inductance and develop explicit design equations. The basic Class-E equivalent circuit is depicted in Fig. 1. The circuit is operated at the carrier frequency $\omega = 2\pi f$, with a conventional 50 % duty cycle. The operation is analyzed in two discrete states. In the OFF state ($0 < \omega t < \pi$), the switch SW is open, whereas in the ON state ($\pi < \omega t < 2\pi$), the switch is considered to be closed. As usual in the Class-E analysis, we will

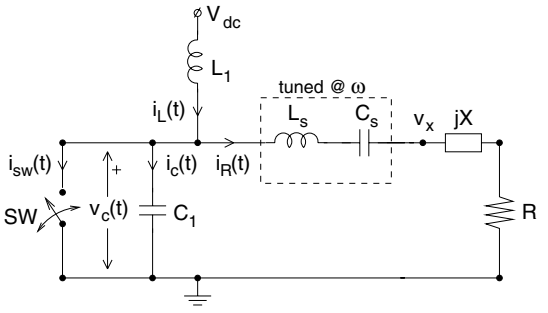

Figure 1: Class-E PA circuit.

assume that the loaded Q-factor of the series L_sC_s resonator is very high, so that only a sinusoidal current at the carrier frequency is allowed to flow

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through the load resistance R. The susceptance of the shunt capacitor C_1 is $B = \omega C_1$ and X represents the excessive (mistuning) reactance. In case of the classic, RFC-based Class-E PA ($L_1 \to \infty$), the design procedure consists of evaluating the three key circuit parameters: the load resistance R, the shunt susceptance B, and the excessive reactance X. The well-known design equations have been many times derived in the literature, and they are given by

$$R = 0.5768\frac{V_{dc}^2}{P_{out}} \quad (1)$$

$$B = 0.1836/R \quad (2)$$

$$X = 1.152R \quad (3)$$

where V_{dc} and P_{out} are the supply voltage and the desired output power, respectively. In case of the Class-E PA with small DC-feed inductance, these equations do not hold anymore. The current $i_L(t)$ will significantly vary throughout the RF cycle, and the circuit operation has to be re-analyzed and solved in time domain. We have performed an exact time-domain analysis of this circuit, by using differential equations and imposing the "soft switching" conditions ($v_c(t) = 0$ and $\frac{dv_c(t)}{dt} = 0$ at the instant of turn-on). A detailed description of such an analysis can be found in [4].

The results of the analysis show that the key circuit parameters R, B and X are transcendent functions of the input parameters (P_{out}, V_{dc}, ω and L_1). Therefore, it is not possible to directly obtain the explicit design equations. In [4], the authors provide a relatively long Mathematica program for calculation of the final circuit elements, but application of this program is a highly impractical and error-prone approach. Furthermore, there is no insight into how the circuit elements are obtained. Therefore, we propose a more practical and intuitive procedure for the circuit design.

At the beginning of the design process, the designer usually has an idea what value of inductance he would like to use for the DC-feeder. Therefore, the reactance of this inductor is known, and it is given by

$$X_{dc} = \omega L_1 \quad (4)$$

On the other hand, an ideal Class-E PA provides a 100 % DC-to-RF efficiency. Therefore, the DC resistance that the circuit presents to the supply source is also known from the PA specifications, and is simply given as

$$R_{dc} = \frac{V_{dc}^2}{P_{out}} \quad (5)$$

Depending on the X_{dc}/R_{dc} ratio, the circuit parameters R, B and X will change their values from those given in equations (1)-(3) for the RFC-based Class-E. We have calculated the values of these three parameters by numerically solving the transcendent circuit equations for a number of different values of X_{dc}/R_{dc}. The results of these calculations are given in Table 1.

X_{dc}/R_{dc}	$P_{out}R/V_{dc}^2$	BR	X/R
∞(RFC)	0.5768	0.1836	1.152
1000	0.5774	0.1839	1.151
500	0.5781	0.1843	1.150
200	0.5801	0.1852	1.147
100	0.5834	0.1867	1.141
50	0.5901	0.1899	1.130
20	0.6106	0.1999	1.096
15	0.6227	0.2056	1.077
10	0.647	0.2175	1.039
5	0.7263	0.2573	0.9251
3	0.8461	0.3201	0.7726
2	1.013	0.4142	0.5809
1	1.363	0.6839	0.0007

Table 1: Class-E circuit elements as functions of the X_{dc}/R_{dc} ratio.

All three parameters are given in a normalized form. The load resistance R is normalized to the supply voltage V_{dc} and desired P_{out}, whereas the shunt susceptance B and the excessive reactance X are normalized to R. For high values of X_{dc}/R_{dc}, the values of R, B and X closely correspond to those for the RFC case, but they significantly change as X_{dc}/R_{dc} is decreasing. In Fig. 2, this variation of the Class-E circuit elements R, B and X is plotted as a function of X_{dc}/R_{dc}. However, the plots are not continuous functions; they are of discrete character, and the curves are actually piecewise linear interpolation of the values given in Table 1.

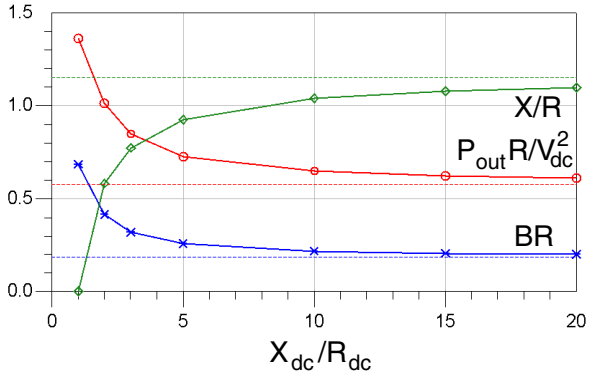

Figure 2: Effect of the finite DC-feed inductance on the Class-E circuit elements.

In order to obtain explicit design equations for the Class-E circuit elements, we have used the Lagrange polynomial interpolation of the numerically

obtained results. From a mathematical point of view, from n pairs of discrete values (x_i, y_i) $i = 1, ..., n$, it is possible to generate a $n-1$-th order polynomial function $y(x)$, such that $y(x_i) = y_i$.

From the plot given in Fig. 2, it can be seen that the area of the most significant variation of the circuit parameters R, B and X is for $X_{dc}/R_{dc} < 5$. Therefore, it is necessary to perform interpolation on this segment with higher density of interpolation points than on the segment where $X_{dc}/R_{dc} > 5$. On the other hand, it is also desirable to limit the number of interpolation points to a reasonable value, in order to obtain relatively simple expressions (i.e. a low order of polynomial). Hence, we have decided to perform interpolation separately on two segments, thus generating two sets of design equations: one for $1 < X_{dc}/R_{dc} < 5$, and the other for $5 < X_{dc}/R_{dc} < 20$. For $X_{dc}/R_{dc} > 20$, the circuit elements values are approaching those for the RF choke case, and thus we will not further consider that segment.

On the segment $1 < X_{dc}/R_{dc} < 5$, we have performed an interpolation with the following four points: $X_{dc}/R_{dc} = \{1, 2, 3, 5\}$. If we denote the ratio X_{dc}/R_{dc} as a variable z, the resulting 3-rd order polynomial expressions are:

$$R = \frac{V_{dc}^2}{P_{out}}(1.979 - 0.7783z + 0.1754z^2 - 0.01397z^3) \quad (6)$$

$$B = \frac{1}{R}(1.229 - 0.7171z + 0.1881z^2 - 0.01672z^3) \quad (7)$$

$$X = R(-1.202 + 1.591z - 0.4279z^2 + 0.03894z^3) \quad (8)$$

On the segment $5 < X_{dc}/R_{dc} < 20$, we have also performed an interpolation with four points, in order to obtain the 3-rd order polynomials which are not too cumbersome, but still provide an acceptable accuracy on the given segment. The interpolation is performed through the following points: $z = X_{dc}/R_{dc} = \{5, 10, 15, 20\}$ and the resulting design equations are:

$$R = \frac{V_{dc}^2}{P_{out}}(0.9034 - 0.04805z + 0.002812z^2 - \\ -5.707 \cdot 10^{-5}z^3) \quad (9)$$

$$B = \frac{1}{R}(0.3467 - 0.02429z + 0.001426z^2 - \\ -2.893 \cdot 10^{-5}z^3) \quad (10)$$

$$X = R(0.6784 + 0.006641z - 0.003794z^2 + \\ +7.587 \cdot 10^{-5}z^3) \quad (11)$$

Design equations (6)–(11) are explicit, relatively simple and can be used for any value of $z = X_{dc}/R_{dc}$ within the corresponding segment. Outside these segments, they are not valid. However, precisely this range of values of X_{dc}/R_{dc} is of the largest practical interest.

It is interesting to study how the utilization of a small DC-feed inductance affects the circuit waveforms in the Class-E PA. We will assume the unity case, i.e. the 1 W PA that is supplied by 1 V DC voltage. In Fig. 3, it is shown how the waveform of $i_L(t)$ changes for different values of X_{dc}/R_{dc}.

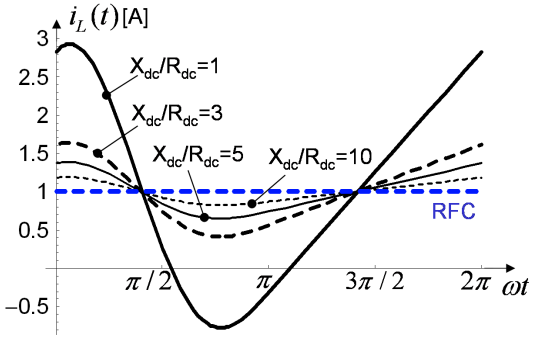

Figure 3: The current through the DC-feed inductance.

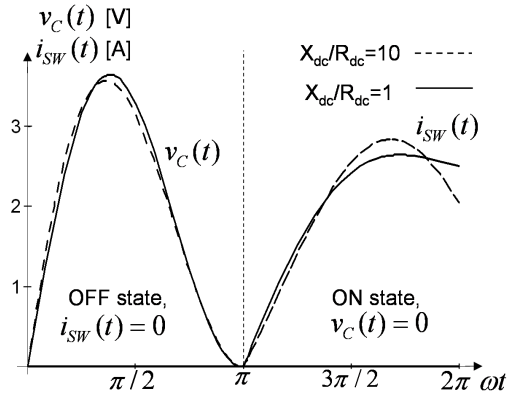

Figure 4: The switch voltage and current waveforms.

From Fig. 3, it can be seen that for low values of X_{dc}/R_{dc}, the DC-feed current can be negative during a certain portion of the RF period. In [4], the authors claim that this operation can present a risk for the active device, due to a reverse breakdown. However, the simulated waveforms in Fig. 4 show that the operation with a very low DC-feed inductance of X_{dc}/R_{dc}=1 does not put much of additional stress on the active device. The peak voltage is only slightly larger than in the RFC-based case, and the peak current is even lower. Thus, this is a perfectly safe operation. However, since the current $i_L(t)$ contains a very significant RF component, special care has to be taken to ensure that the the DC-supply source is properly bypassed by a low-ESR capacitor.

In low-voltage, high-frequency applications, the utilization of a finite DC-feed inductance has several major benefits. First, it results in a higher load resistance in comparison to the RFC case. This effect makes easier the design of low-loss matching networks, since the designer typically needs to transform a standard 50 Ohm termination to the load resistance of several Ohms. Furthermore, the excessive inductance X is also lower, and the shunt susceptance B is increased. This increase of the shunt susceptance is particularly useful, as it extends the maximum frequency limitation of the device imposed by its output capacitance.

3 Design example

In this section, the obtained design equations will be verified with the following design example. The goal is to dimension the Class-E circuit elements for the following PA specifications: V_{dc}=3V, P_{out}=1W, f=2GHz and we will assume that we want to use a DC-feed inductance of L_1=2nH. From (5), we find R_{dc}=9Ω, and from (4) and the initially chosen value for L_1, we obtain X_{dc}/R_{dc}=2.793. Therefore, we need to use equations (6)–(8), suitable for interpolation on segment $1 < X_{dc}/R_{dc} < 5$. By setting $z = X_{dc}/R_{dc} = 2.793$ and applying (6)–(8), we obtain the following values: R=7.822Ω, B=0.04208S, and X=5.883Ω. The calculated values of B and X correspond to the shunt capacitance of 3.349pF and series inductance of 0.468nH, respectively.

A schematic of the designed and simulated Class-E circuit is displayed in Fig. 5. The inductance L_m and capacitance C_m transform the 50Ω load to the desired value of R=7.822Ω, while L_s and C_s form a high-Q series resonator. In practice, inductances L_s, L_x and L_m can be lumped into a single inductor, and L_1 can be implemented by a bondwire inductance. The circuit has been simulated by transient analysis in ADS, and the following results are obtained: P_{out}=1.02W and η=97.4 %. The simulated switch voltage and current waveforms are displayed in Fig. 6 and they indicate a near-perfect Class-E operation. A small disturbance in the waveforms can be ascribed to the parasitic switch resistance R_{SW} and the limited Q-factor of the output network, as well as to the small error of the interpolation polynomial.

4 CONCLUSIONS

In this paper we have presented novel, explicit design equations for Class-E power amplifiers with finite DC-feed inductance. Numerically obtained results are interpolated by Lagrange polynomials of the third order. The proposed method has been verified by simulation, and the agreement with the theoretical expectations is excellent.

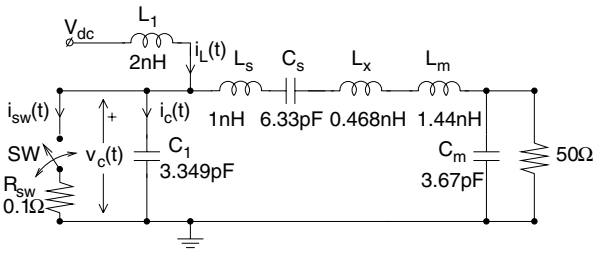

Figure 5: The Class-E PA for 2 GHz.

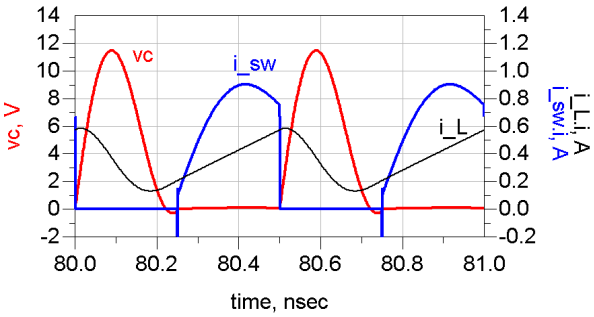

Figure 6: The switch voltage and current waveforms and the DC-feed inductance current.

Acknowledgments

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