DESIGN AND OPTIMIZATION OF A LOW JITTER CLOCK-CONVERSION PLL FOR SONET/SDH OPTICAL TRANSMITTERS

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Abstract

A robust clock-conversion PLL is presented for use in optical transmitters. The alignment-free PLL has a fully integrated loop-filter, rail-to-rail high-ohmic-input V/I-converter and a double-integrator oscillator which leads to small chip-area. The PLL frequency response is optimized for minimisation of the jitter of the output signal. All critical building blocks are designed for 2.4 V, in order to allow stacking of a voltage stabiliser with good power supply rejection ratio. The 155/622 MHz PLL is realized in BiCMOS technology with 18 GHz cut-off frequency. The PLL is evaluated under temperature conditions ranging from -40 °C to 85 °C and found SONET/SDH compliant. Maximum transmit jitter is 4.4 mUI rms. Active chip area is 1.65 mm^2. The dissipation is 65 mW with a 3.0 V power supply voltage.

1 Introduction

One of the key building blocks for optical transmitters is the Clock-Conversion Phase-Locked Loop (CC-PLL). In the transmitter, a parallel input data stream is multiplexed into non-return-to-zero serial output data. The serial data then feeds the laser driver circuitry, and is finally transferred into the optical domain by a laser. The parallel-to-serial data conversion requires the parallel byte-clock to be converted into a serial, low-jitter bit-clock at the transmission speed.

A major part of the optical network market follows the ITU SONET/SDH standard [1, 2]. For an optical transmitter to be SONET/SDH compliant, the total jitter of the serial data in the *optical* domain must be less than 10 milli Unit Interval (mUI) rms.[1] Therefore the "jitter budget" of 10 mUI rms must be shared between the parallel-to-serial converter, the laser-driver and the laser. In practice, each of these blocks are specified to generate no more than half of the total allowed jitter power. This leads to a jitter specification for the clock-converter alone of 7.1 mUI rms (i.e. 3 dB below 10 mUI rms).

Irrespective of the data rate, several design requirements are important for a Clock-Conversion PLL suitable for SONET/SDH applications. First of all, the CC-PLL must satisfy the SONET/SDH standards under all temperature (ranging from -40 °C to 125 °C), process and supply-voltage conditions. Secondly, the CC-PLL must be robust against interference from supply and substrate noise. Digital I/O will be on the same die, hence the power supply rejection ratio (PSRR) and substrate noise rejection ratio of the CC-PLL needs to be high. Thirdly, especially for the lower data rates where the market is established, the CC-PLL design should aim for minimum cost. This translates into a fully integrated loop-filter and an alignment-free implementation, with minimum chip-size using a standard high-volume IC process. This paper presents a robust CC-PLL realization for 155 Mb/s and 622 Mb/s data transmission over optical fiber, which complies with the requirements mentioned above.

First, the architecture of the CC-PLL is highlighted in Section 2. Then the V/I converter and oscillator design are described in Section 3, with a focus on VCO gain minimisation and low phase noise design. Section 4 presents the overall PLL design and optimization procedure for low-jitter performance. After that, measurement results are presented in Section 5, followed by the conclusions.

2 Clock conversion architecture

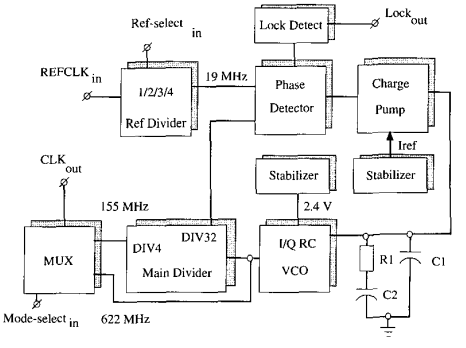

Figure 1. Clock conversion architecture.

The block-diagram of the CC-PLL architecture is shown in Fig. 1. The function of the CC-PLL is to convert the 19.44 MHz byte-clock of the parallel data stream

[1] For a 622 Mb/s transmitter, the jitter is evaluated in a bandwidth of 12 kHz to 5 MHz. These limits change as function of the bit-rate. For details see [1, 2]

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into a serial bit-clock of 155 MHz or 622 MHz.

The phase detector of the CC-PLL works on a reference frequency of 19.44 MHz. If a multiple of this reference frequency is used it is divided down to 19.44 MHz and hence the loop needs to be optimized for only one reference frequency. Connected to the phase detector is the Lock Detect which signals when the PLL is in lock. The output multiplexer selects either the 622 MHz or the 155 MHz bit-clock, which is derived from the 622 MHz signal through division-by-4. To minimize sensitivity to external interference (e.g. power supply noise) the VCO and charge-pump were given separate stabilizers. Furthermore, the loop filter has been fully integrated.

The main design consideration was robustness, so that the PLL can acquire lock and provide a clean output signal under all processing and temperature conditions. These aspects are discussed in the next sections.

3 VCO design

The phase noise of the VCO in the CC-PLL has a direct influence on the jitter generation. PLL system simulations, discussed in the next session, showed that a VCO single-sideband noise $\mathcal{L}_{vco}(f_m)$ of -106 dBc/Hz at 2 MHz offset of the 622 MHz carrier would suffice. With a power budget of 10 mA this phase noise specification can be met with a two-integrator oscillator [3]. (An LC oscillator would save power and provide a better frequency stability w.r.t. temperature and process variations, but at the cost of a substantial increase in chip-area.) The circuit implementation of the two-integrator current-controlled oscillator (CCO) is shown in Fig. 2.

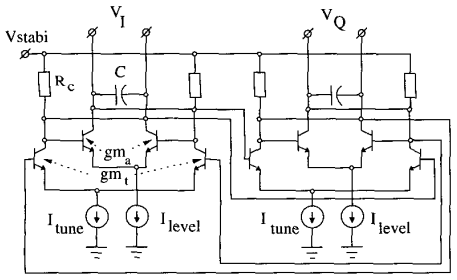

Figure 2. Circuit implementation of the two-integrator oscillator.

The differential pair gm_t in each stage and capacitor C implement the integrator. Capacitor C is shown lumped for clarity, but it is implemented using the device parasitics of the differential pairs. The losses which are formed by the collector resistors (R_c) and input resistance of the differential pairs are compensated by cross-coupled pair gm_a. This differential pair implements a negative resistance. Neglecting second order effects, the oscillation frequency f_{osc} is equal to

$$f_{osc} = \frac{I_{tune}}{8\pi V_T C}, \qquad (1)$$

where $V_T = kT/q$ is the thermal voltage. A feature of the CCO is that it provides quadrature (I/Q) signals, since each stage provides exactly 90° phase shift. The oscillator supply voltage V_{stabi} is 2.4 V and is provided by a voltage reference based on the band-gap principle. The voltage reference improves the PSRR. The voltage reference is designed with a low-pass noise characteristic with a 3 dB bandwidth low enough to not affect the phase noise in the jitter bandwidth of interest (12 kHz to 5 MHz).

The integrated loop-filter output of the CC-PLL is a voltage, hence a V/I converter is needed to convert this voltage into tuning current I_{tune}. This V/I converter must have a high-ohmic input to minimize reference breakthrough caused by leaked charge from the loop-filter [5]. It also should use the available voltage swing, about 0.3 V to 2.1 V (0 to 2.4 Volt ± a saturation voltage for the charge pump) to minimize the tuning constant K_{VCO}. Modulation theory shows that the carrier-to-noise ratio $CNR(f_m) = (2\ f_m)/(V_{noise}\ K_{VCO})$. Therefore the CNR at offset frequency f_m, as result of loop-filter noise V_{noise}, can be improved by minimizing K_{VCO}.

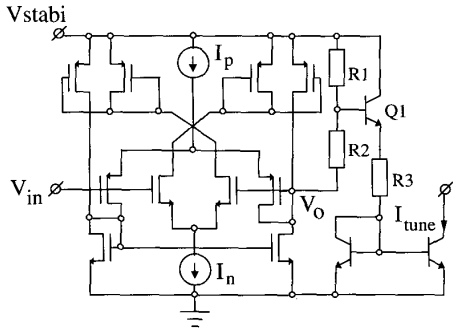

Figure 3. VI-converter schematic.

Fig. 3 shows the circuit implementation of the realized V/I-converter. The left half of the circuit is a CMOS rail-to-rail buffer which provides the high-ohmic input [4]. In order to maintain the rail-to-rail and linear transfer character, the output voltage V_o is mapped onto a voltage between 0.7 V and V_{stabi} (2.4 V). This provides room for the base-emitter voltage of Q_1, the voltage drop across R_3 and one saturation voltage of the current source. Transistor Q_1 implements temperature compensation: the V/I converter has a positive temperature coefficient which compensates the oscillation frequency dependence on V_T, see (1). The V/I-converter voltage V_{stabi} is supplied by the same reference generator used for the CCO.

Fig. 4 shows the oscillation frequency for slow, nominal and fast processing conditions, and temperatures of -40, 25 and 125 °C. In this simulation the V/I-converter input voltage V_{in} was set to 1.2 V. We observe that temperature compensation is effective, and that most frequency deviation arises from process variations. However, additional simulations showed that in all cases the VCO can be tuned to the required 622 MHz. Simulated K_{VCO} varies

less than a factor 3 between 95 MHz/V and 220 MHz/V, under all processing and temperature conditions.

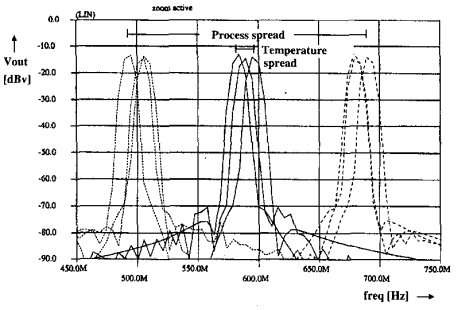

Figure 4. Simulated free-running oscillator frequency, for different temperature situations and process parameters: slow, nominal and fast.

4 PLL design

The PLL design presented in this section aims at minimizing the jitter of the CC-PLL output signal. The jitter is found by integration of the SSB phase noise power density $\mathcal{L}(f_m)$ [dBc/Hz], for offset frequencies f_m ranging from 12 kHz to 5 MHz:

$$\text{jitter} = \frac{1}{2\pi}\sqrt{\int_{12k}^{5M} 2 \cdot 10^{\frac{\mathcal{L}(f_m)}{10}}\, df_m} \text{ [UI rms]}. \quad (2)$$

Table 1 presents the jitter of the free-running oscillator for three different situations of gain and phase-noise performance. The jitter specification of 11.7 mUI rms is not met under any circumstance. Therefore, the jitter must be minimized by wide-band locking the VCO signal to the clean 19.44 MHz reference clock signal.

Table 1. Jitter Free-running Oscillator.

Situation	Spectral Purity @ 2MHz [dBc/Hz]	Jitter [mUI rms]
Nom. gain/noise	-102	20.7
Low gain/noise	-104	16.6
High gain/noise	-96	41

For phase-noise reduction, the choice $f_c = f_{xover}$ for the PLL open-loop bandwidth f_c (also known as 0 dB cross-over frequency) leads to minimized jitter of the loop. The frequency f_{xover} is the offset frequency where intersection of the free-running phase noise power density from the VCO and from the "PLL blocks" (dividers + PFD/CP) occurs [5]. The numerical value of f_{xover} is

$$f_{xover} = \frac{f_r \cdot 10^{\frac{\mathcal{L}_{vco}(f_r) - \mathcal{L}_{eq}}{20}}}{N}, \quad (3)$$

where $\mathcal{L}_{vco}(f_r)$ is the free-running, SSB VCO phase noise power density (in dBc/Hz) at a given reference offset frequency f_r, $\mathcal{L}_{eq}$ is the equivalent synthesizer phase noise floor at the input of the phase detector, and N is the main divider division ratio. With the present PLL, $\mathcal{L}_{eq} \simeq -130$ dBc/Hz, $\mathcal{L}_{vco}(2MHz) \simeq -102$ dBc/Hz and $N = 32$, which leads to $f_{xover} \simeq 1$ MHz. Fig. 5 shows the simulated closed-loop SSB phase-noise spectral density of the output signal, with $f_c = 1$ MHz. Note that the "PLL blocks" dominate at offset frequencies smaller than f_c, and the VCO dominates at frequencies larger than f_c.

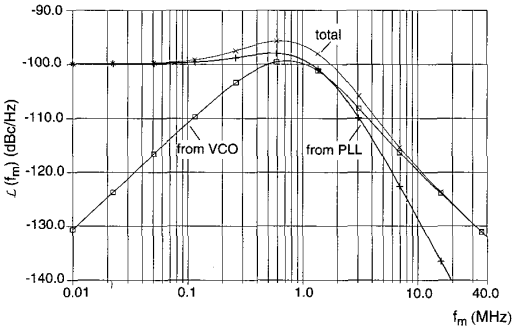

Figure 5. Simulated SSB phase noise power density with $f_c = f_{xover}$, depicting the contribution from the different phase noise sources.

The loop-filter impedance level was dimensioned to provide an open-loop bandwidth f_c of 1 MHz, with a nominal charge-pump current I_{CP} of 120μA. The jitter in closed-loop situation is depicted in Fig. 6, as function of I_{CP}. For the nominal situation, the jitter is reduced from 20.7 mUI rms to 4.7 mUI rms, and worst-case from 41 mUI rms to 6.9 mUI rms.

The total capacitance of the second-order loop filter is 55 pF, with a stabilizing resistor R_1 of 9 kΩ, see Fig. 1. The PFD/CP circuits are based on the designs presented in [5].

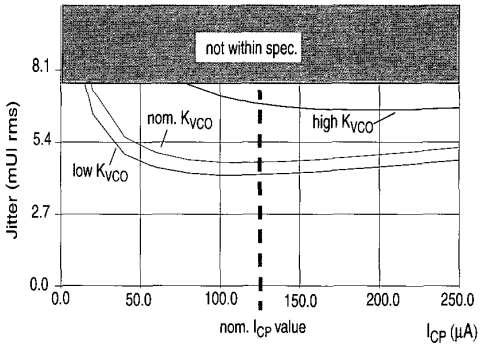

Figure 6. Jitter of the CC-PLL, for different values of charge pump current and VCO conditions.

5 Experimental results

Measurements were performed on 10 packaged samples (QFP 64-pins package), using an automated measurement setup. The presented results are device averages or minimum and maximum measured values. The CC-PLL operates with a supply voltage ranging from 5.0 V down to 2.7 V. Reported measurements are performed with a 3.0 V supply voltage. In that case the nominal dissipation (at 25 °C) is 65 mW.

Table 2. Jitter Clock Conversion PLL.

Ambient Temp. °C	Min. Jitter [mUI rms]	Max. Jitter [mUI rms]
-40	3.8	4.2
25	3.6	4.4
85	3.7	4.3

Most critical is the jitter performance of the CC-PLL. During the measurements digital I/O cells on the same silicon die were active. Measurement results in Unit Interval rms are given in table 2. Under all conditions the rms jitter is more than 4 dB lower than the 7.1 mUI rms specification. Since the ITU specification refers to the output jitter of the total transmitter, effectively as much as 9 mUI rms jitter can be allowed for the laser driver and laser, since jitter adds power-wise.

Table 3. Lock Range Clock Conversion PLL.

Ambient Temp. °C	Min. Freq [MHz]	Max. Freq [MHz]
-40	520	870
25	550	855
85	548	820

Table 3 shows the lock range of the I/Q RC oscillator for three temperatures. The temperature compensation implemented in the V/I-converter is effective in stabilizing the lock range. Without alignment, the oscillator is able to acquire lock across the whole temperature range.

The CC-PLL spectrum at 622 MHz with at 19.4 MHz reference clock is shown in Fig. 7. Careful design of the charge-pump and loop-filter led to a spurious reference breakthrough of less than -56 dBc.

Fig. 8 shows the chip micro-graph. The CC-PLL has a chip area of 1.65 mm^2.

6 Conclusion

An alignment-free clock conversion PLL for use in 155/622 Mb/s optical transmitters has been realized. The loop has been designed to provide optimal jitter performance. The PLL has an integrated loop-filter, rail-to-rail V/I converter and two-integrator current-controlled oscillator. Maximum jitter in a temperature range from -40 °C to 85 °C was measured to be 4.4 mUI rms, which is 4 dB lower than the ITU SONET/SDH specification. The PLL occupies 1.65 mm^2 and is realized in an 18 GHz f_T BiCMOS. With 3.0 V the dissipation is 65 mW.

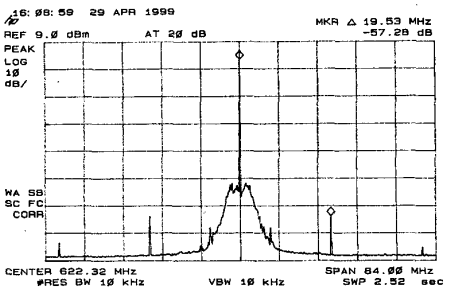

Figure 7. Spectrum of the clock-conversion PLL.

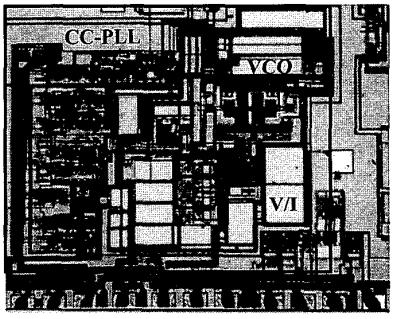

Figure 8. Chip micro-graph.

Acknowledgement

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