Design of Flexible RF Building Blocks-A Method for Implementing Configurable RF Transceiver Architectures

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Abstract

In today's world, new communication standards evolve fast, putting a significant burden on set makers and RF IC designer houses to bring integrated and cheap solutions quickly into the market place. The shift towards flexible RF systems that can support a range of applications via adjustability and re-usability is a solution to these problems. In this paper an approach for design of adjustable and programmable RF building blocks is represented as a basis for adding flexibility and multi-standard capability to transceiver front-ends. The design approach is based on generating a library of reusable, configurable RF building blocks and a structured, economical method for implementing transceivers using these building blocks.

1. Introduction

The number of systems that use radio links is increasing quickly. At the same time, the number of standards for such systems is increasing very quickly as well. For example Bluetooth and ultra-wideband (UWB) standard support Wireless Personal Area Network (WPAN) systems. Wireless Local Area Network (WLAN) systems are based on IEEE 802.11a, 802.11b, 802.11g standards. IEEE 802.16a, IEEE 802.16d and IEEE 802.16e standards support Wireless Metropolitan Area Network systems. Among the cellular standards (Wide Area Network, WAN) are GSM in 450 MHz, 480 MHz, 850 MHz, 900 MHz (in standard, extended and railway variations) bands, DCS 1800, PCS 1900, with or without GPRS and EDGE extensions, AMPS, IS-95, IS-98, IS-136, UMTS, PDC in high and low bands, CDMA2000 and TD-SCDMA. These are just a subset of the most popular and relatively recent standards.

Such a fast growth in wireless communications standards creates new challenges for RF system and circuit designers. The most obvious challenge is the development of systems and components for each of these different standards in time and with limited resources. Using typical numbers for RF IC design projects, the overall development timeline of a RF system is estimated in [1] and it takes more than 10 months. With N radio applications, however this will require N*(RF design timeline). Since the number N is becoming so big, the development of the individual radio links in the time and with the limited resources is becoming more and more difficult.

One the other hand, one of the most recent and interesting challenges is the trend towards integration of multiple radio links. The integration of multiple radio links might be required either for different applications (e.g. Bluetooth in a WLAN application) or for compatibility with different systems at various locations (e.g. different types of cellular phone networks in different countries). A multifunctional radio link is valuable only if it is less expensive and/or smaller than simply putting multiple radio components next to each other. In addition it has to have acceptable performance and low power dissipation. One way to reduce the cost is to achieve a high level of integration and to eliminate the external components as much as possible. Another way to reduce the cost of the multiple function systems is to reuse building blocks among different radio links in order to limit chip area to a minimum.

Several methods are recently considered to solve these problems. They are discussed in more detail in section 2. Section 3 focuses on the system aspects of configurable RF transceiver architectures. These include: defining a common architecture, defining a multi-standard architecture and designing adjustable and configurable building blocks.

2. RF design methods

Several methods to solve the previous mentioned problems are presented in fig. 1, [1]. They are varying from current methods as full-custom design and different methods of reuse, to a full software radio consisting of an antenna, data converters and signal processing in software. These methods have different trade-offs with respect to cost and flexibility.

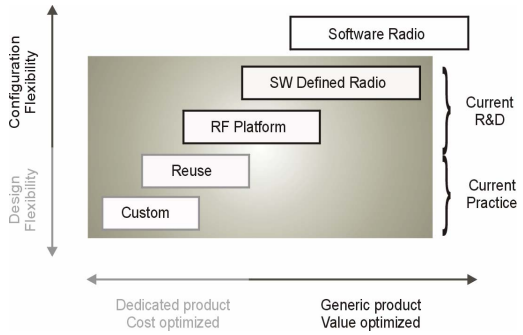

Figure 1: RF design methods

The custom design method is a currently used method where final design is fully optimized to a dedicated

product. In this case flexibility of the final design is very low. Although design is cost optimized for a specific product, the investment in the effort and the time needed to develop N transceivers is larger than in the other methods. Moreover, since the multifunctional transceiver is integrated by simply putting multiple radio components next to each other, the chip area is not optimally used.

The reuse method reduces only the development time and effort of transceivers. In this case developed circuits are reused for new radio links without changing their internal implementation. The final system is integrated by combining suitable predesigned building blocks. This can result in a transceiver with a higher cost since it is not optimized for a given product. However, the development time is shorter in comparison to the full custom design. In practice, the reused RF building blocks are modified and optimized rather than reused as is. This is done to have a better trade-off between time & effort invested to develop a system and cost & performance of the final system. In the future, it is expected that more strict and formal rules will be defined within the reuse method. This should bring the reuse method to the higher level of acceptance for the designer.

The Platform–based method is a trade-off between flexibility and cost optimization. Platform–based transceivers are assembled from pre-existing, configurable building blocks through system-in-package (SiP) integration, [1]. The reason for implementing the system through SiP integration is that SiP fabrication tends to be faster than the SoC (System-on-Chip) fabrication. This will reduce the time-to-market. Moreover, for different building blocks appropriate technologies and design approaches can be used. Hence, the achieved transceiver performance can be very high. The granularity of the building blocks is a trade-off between flexibility and cost. Small building blocks such as individual transistors and passive components enable more flexibility. However, if the building blocks become so small that the number of connections becomes very large, the building blocks become bond-pad limited. In addition to increasing the die costs, this might increase the assembly cost as well due to many interconnections required. Larger building blocks can be more cost efficient, but they are usually less flexible. When the number of building blocks and the number of connections between the building blocks is optimal, the cost tends to be similar or slightly higher than the cost for SoC integration. It is expected that, when the market matures, next generations of a product will be developed using more cost optimized methods (reuse, custom design).

Software defined radios aim to provide a single transceiver with multiple functions, [2]. In software define radios signal processing is done partly in analog hardware and partly in digital hardware. In this case the properties of the radio can be adjusted through software without changing the hardware. The properties of the transceiver can be changed after the radio is fabricated. Moreover, it is possible to change the properties during operation, to deal with the changes in the environment, properties of the signal or to communicate in a different standard mode. While these systems are very flexible, the cost and power dissipation are higher. However, if the number of supported bands and modes is increasing, more resource sharing is possible. This will compensate for the extra complexity and cost. The disadvantages are likely to decrease in the future due to improvements in the technology.

Software radios consist of an antenna, an Analog-to-Digital converter (ADC) and a Digital Signal Processor (DSP). After the data converter all signal processing is done in software. The properties of software radios can be changed during operation as it is the case with software defined radios. The complexity of the ADC and software result in extra cost and/or power dissipation. However, this may be compensated when the number of the supported modes and bands is increasing. For now, due to the limitations of ADCs, software radios are still further in the future.

The Platform-based design method and the software defined radios method might be an intermediate solution to the software radios in terms of flexibility and cost/value optimization. These two methods are a subject of research projects. For both methods some issues have to be solved. They are discussed in the next section.

3. Multi-standard front-end design

A number of critical issues at RF design level need to be solved when a flexible, multi-standard receiver is designed. These include: defining a common architecture, defining a multi-standard architecture and designing adjustable and configurable building blocks. The common architecture needs to support all the standards within the multi-standard receiver with acceptable cost, size and performance. The multi-standard, multi-band architecture has to be developed by using the common architecture and configurable building blocks. Adjustable and configurable building blocks that can support all the standards within the multi-standard receiver have to be created.

These critical points will be discussed in the next sub-sections.

3.1 A common architecture

Several front-end architectures are present in literature. They range from an RF sampling front-end architecture supporting software defined radios, through low-IF and zero-IF front-end architectures with a direct conversion, to low-IF and zero-IF front-end architectures with a double conversion.

These architectures have different trade-offs with respect to the minimization of the number of the building blocks and the translation and distribution of the system specifications to building block specifications. This has to be done in such way that their design and implementation are relatively easy. In the RF sampling front-end architecture ADC is connected to the antenna. So, the minimal number of the building blocks is used and building block specifications can be calculated and optimized more easily. However, a high frequency and a large dynamic range of received signals cause a high

power consumption of the ADC (in the order of several Watts, [11]). In the low-IF and the zero-IF front-end architectures with a double conversion the building block specifications are more relaxed, [4], which results in easier design and implementation of the blocks. However, the time to calculate and optimize the building block specifications will increase.

Hence, the selection of a common front-end architecture is a key aspect in a multi-standard, multi-band system design. The common architecture needs to support all transceivers with acceptable cost, size and performance. Based on the state-of the art in [2] it was determined that the zero-IF architecture is the most suitable solution for UMTS and wireless LANs and the low-IF architecture is the most suitable solution for Bluetooth and GSMs, [2]. Hence, it was shown, [1], [2] and [3], that the zero-IF/low-IF architecture with a direct-conversion can be used as a common architecture for most of the wireless applications, (see fig. 2).

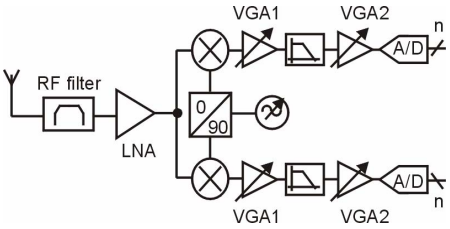

Figure 2: A zero-IF/low-IF architecture

For the low-IF architecture, we assume that the I and Q path will be combined in the digital domain in order to perform the image suppression. The multi-standard, multi-band architecture is based on this common architecture.

3.2 Multi-standard, multi-band architecture

The simplest multi-standard radio can be realized by putting multiple, individual radio components next to each other. However this is not a cost-effective solution, and with an increasing numbers of radio links it becomes no longer feasible. In a multi-standard receiver the chip area should be optimally used. This means that the transceiver architecture has to enable building block reuse and hardware sharing. In a multi-functional system, concurrency of the applications has to be investigated as well. Standards that do not need to be covered at the same time can share the same hardware.

Most recent published receivers for multi-mode applications, [4] and [5], propose the implementation of multi-band cellular phones for the GSM standard (850, 900, 1800 and 1900 MHz). The chosen architecture in these examples is zero-IF both for CMOS [4] and BiCMOS [5]. In [4] there are two mixers, one for the 850 and 900 MHz bands, and one for 1800 and 1900 MHz bands, and they are the first building blocks, in the receiver path to be shared. In [5] the low noise amplifiers (LNAs) consist of four differential transconductors recombined through a cascade stage into two resistive loads, one output resistive load for 850 and 900 MHz, and the other output resistive loads for 1800 and 1900 MHz. The output loads of the LNAs are the first blocks in the receiver that are shared. In wireless LAN applications there are currently many examples of multi-standard solutions. Recently a dual band CMOS front-end for WLAN applications is proposed, [6]. In this example a dual band LNA with two inputs is used for two different bands at 2.4 GHz and 5.15 GHz. Here a first shared building block is the LNA. However, the restriction of this application is that one LNA can be shared within only two applications.

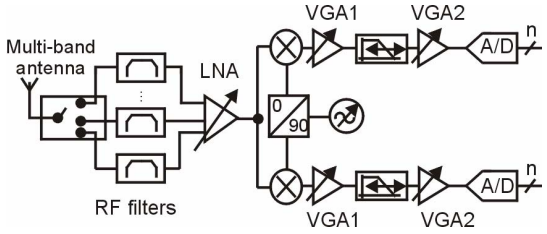

Figure 3: Proposed multi-standard architecture

In fig. 3, [2], the block diagram of the fully integrated multi-standard architecture is shown. This choice allows maximum hardware sharing in the receiver chain. Therefore, the receiver requirements deserve a particular note. Since, the different standards require different front-end performance, the easiest solution would be if the front-end is designed in a way that satisfies the most critical specifications. However, with this approach, the cascaded performance will be too demanding. This suggests that the front-end should be configurable for a specific standard in the reception. Hence, reusable and configurable building blocks that are optimized for use in these architectures have to be created.

In the case of concurrent applications the same transceiver chain has to be doubled.

3.3 Configurable and reusable building blocks

The different standards require different front-end performance, [2]. The cascaded performance of a multi-standard front-end will be too demanding when the front-end is design to satisfy the combination of the most critical specifications for each standard. This suggests that the building blocks of the front-end need to be adjustable and configurable. The multi-standard transceiver with adjustable and configurable building blocks is valuable only in the case if it is less expensive and/or smaller than simply putting multiple radio components next to each other, while simultaneously achieving acceptable performance and low power dissipation. This requires a careful design of configurable and reusable building blocks. This in turn, is strongly related to the design space of a building block and the performance space that can be covered by the adjustable circuit.

In order to choose an appropriate topology for a given specification space, particular investigations of the topology have to be performed. First, DC limitations of the topology have to be determined, which means all transistors have to be in the required region of operation. Than a maximal range for each design parameter has to be determined. In this way the design space of the topology will be determined.

From the design space then, the performance space of the topology has to be determined. The performance space can be estimated by presenting each circuit performance as a function of the design parameters:

$$\begin{aligned} &Circ.Perform.1 = f_1(des.param1,...,des.paramN) \geq Spec.1 \\ &... \\ &Circ.Perfom.N = f_N(des.param1,...,des.paramN) \geq Spec.3 \end{aligned} \quad (3)$$

where *Des.param.1*, …, *des.param.N*, are design parameters of the building block such as bias currents, transistor sizes, resistors, capacitors, inductors, *Circ.Perfom.1*, …, *Circ.Perfom.N* are circuit performance such as *Gain*, *Noise Figure (NF)*, *IIP2*, *IIP3*, and so one, $Spec_1$, , $Spec_N$ are the specifications that must be satisfied, and $f_1, f_2, \ldots, f_N$ are nonlinear functions of the design parameters. Formulating these functions can be a complex task and usually the exact performance space is determined by simulations.

If the performance space of the investigated topology can not cover the desired specification space, some techniques have to be applied to this topology in order to extend the performance space. If the performance space of this topology can not still cover the desired specification space a new topology need to be investigated. When the performance space of the investigated topology can cover the desired specification space methods to vary topology performance should be applied. These methods will introduce performance degradation and will narrow the performance space of the building blocks. Hence, these methods should be properly chosen, such that the performance degradation is minimized.

Finally, if the topology with adjustable performance cannot cover the specification space due to performance degradation a new topology has to be selected. The adjustable building block is complete if the adjustable topology can cover the specification space.

An investigation of a design space of a Gilbert cell mixer is done in [7]. In order to vary the topology performance discrete tuning is applied to the basic Gilbert cell mixer, and a Gilbert cell mixer with a discretely adjustable performance space is derived (see fig. 4). More detailed explanation of the Gilbert cell mixer with a discretely adjustable performance space is given in [7].

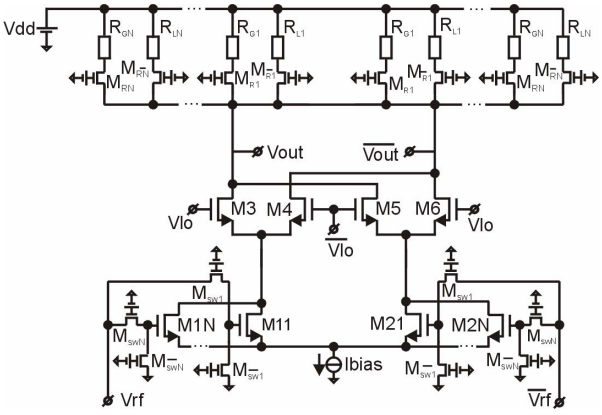

Figure 4: A Gilbert cell mixer with a discretely adjustable performance

In order to estimate degradation of performance the fixed Gilbert cell and the Gilbert cell mixer with a discretely adjustable performance space are simulated, by using the circuit simulator SpectreRF in CMOS 0.25um technology. For this specific case the transconductance stage of the discretely adjustable Gilbert cell consists of 3 differential pairs where M_{11} has *W/L=50/0.25*; M_{12} and M_{13} have *W/L=100/0.25*. M_{12} and M_{13} could be switch *ON* and *OFF*. The combination of transistor sizes, a bias current (I_{bias}) and load resistors used in this example are presented in Table 1. The sizes of switches are: $M_{sw,i}$ has *W/L=100/0.25*, $M_{\overline{sw,i}}$ has *W/L=10/0.25*, and $M_{R,i}$ and $M_{\overline{R,i}}$ have *W/L=100/0.25* (*W* and *L* are width and length of a transistor). $R_{G,l}$ is the load resistor for which a maximum voltage gain is achieved, and $R_{L,l}$ is the load resistor for which the maximum input-referred *IIP3* is achieved. The fixed Gilbert cell is simulated separately for each combination.

Table 1: The combinations of the design parameters for the discretely adjustable Gilbert cell

transistor sizes	50um	150um	250um
$\mathbf{I_{bias}}$=1mA	R_{G1} =2.5K R_{L1} =2K	R_{G1} =2.5K R_{L1} =2K	R_{G1} =2.5K R_{L1} =2K
$\mathbf{I_{bias}}$=5mA	R_{G2} =550 R_{L2} =350	R_{G2} =550 R_{L2} =350	R_{G2} =550 R_{L2} =350
$\mathbf{I_{bias}}$=10mA	R_{G3} =180 R_{L3} =100	R_{G3} =250 R_{L3} =100	R_{G3} =250 R_{L3} =100

The simulated ranges for a voltage gain, a *NF* (the SSB NF is simulated at a 50Ω source impedance) and an *IIP3* of the fixed Gilbert cell and the discretely adjustable Gilbert cell are given in Table 2.

Table 2: Simulation results at 2.5GHz

	Gain [dB]	**NF [dB]**	**IIP3 [dBm]**
Fixed Gilbert cell	Max =16 Min =-2	Max =14 Min=7	Max=12 Min =-8
Adjustable Gilbert cell	Max =15 Min=-2	Max =16 Min=9	Max =11 Min=-8

From the obtained results, it can be concluded that significant flexibility at a relatively low (1 or 2dB) degradation of performance compared to a full custom design is achieved.

Another example of adjustable RF building blocks, a Gilbert cell mixer with a continuously adjustable performance is shown in fig. 5. In this example one extra stage consisting of transistors M_{11} and M_{22} is added to the basic Gilbert cell, in order to extend the performance space. Moreover, the performance space can be continuously varied by changing the bias current I_{bias2}. A more detailed explanation of this circuit is given in [8].

The measured (the solid line) and simulated (the dashed line) results of this continuously adjustable Gilbert cell are presented in fig. 6. The input signal is set to 2.5GHz, while the output signal is measured at an IF-frequency of 2MHz.

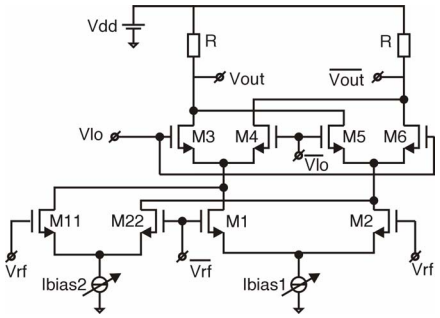

Figure 5: A Gilbert cell mixer with a continuously adjustable performance space

A SSB *NF* is measured at a 50Ω source resistance. The differential *LO* voltage swing is V_{lo}=500mVp, the supply voltage is 2.5V, I_{bias1}=3.3mA, R=500Ω, L_{d1}=L_{d2}=L_s=0.25um (L_{d1} is length of M_1 and M_2; L_{d2} is length of M_{11} and M_{22}) W_{d1}=100um, W_{d2}=40um, W_s=80um (W_s and L_s are width and length of M_3, M_4, M_5 and M_6). The die photo of this realized topology is shown in fig. 7. The active chip area is 180um x 210um.

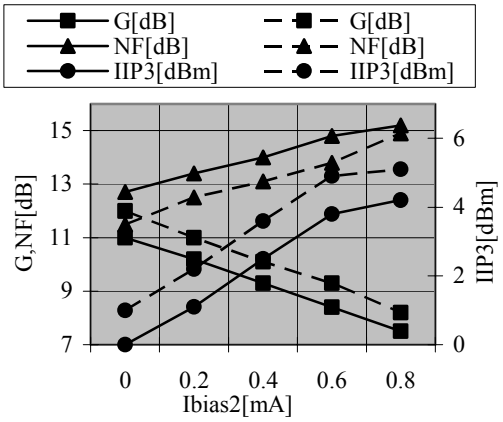

Figure 6: Measured (solid line) and simulated (dashed line) results

The basic Gilbert cell was also realized. For the same design parameters (as the continuously adjustable Gilbert cell) and *Ibias1*=3.3mA a voltage gain of 13dB, a *NF* of 12dB and an *IIP3*of 1dBm are obtained. Both circuits are implemented in CMOS 0.25um technology.

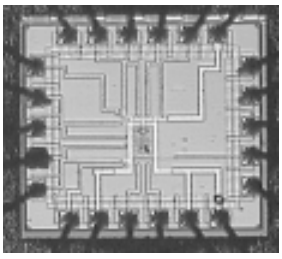

Figure 7: Die micrograph of the adjustable Gilbert cell

For discrete as well as for continuous performance space variation it can be concluded that flexibility with a relatively low (1 or 2dB) performance degradation compared to a full custom design is achieved. Hence, making multi-standard RF systems that can support a range of applications through adjustability and re-usability could well be feasible option. The total cost of complete flexible multi-standard systems is yet to be determined and a subject of on-going research.

Some other interesting examples of configurable circuits are presented in [9] and [10].

4. Conclusions

In this paper, a review of RF design methods for the development of transceivers for different standards is presented. The current custom and reuse design methods are not sufficient to support the recent, challenging multi-standard trend. The Platform-based design method and the software defined radio method are a promising solution in terms of flexibility and cost/value optimization. Both methods require a structural method of designing adjustable and configurable building blocks and implementing them in a multi-standard architecture. Hence, in this paper the approach for generating a library of reusable, configurable RF building blocks and a structured method for implementing transceivers using these building blocks are presented. Some examples of adjustable building blocks are presented, as well. From the obtained results, it was concluded that flexibility with a relatively low (1 or 2dB) performance degradation compared to a full custom design is achieved. Hence, it was shown that flexible multi-standard RF systems that can support a range of applications through adjustability and re-usability could well be a cost-effective approach for the realization of flexible multi-standard transceivers.

5. REFERENCES

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