A 375 mW, 2.2 GHz Signal Bandwidth DAC-based Transmitter with an In-band IM3 < −58 dBc in 40 nm CMOS

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***Abstract*— A 40 nm DAC-based CMOS wideband transmitter (WBTX) for cable applications is presented. It has a 2.2 GHz signal bandwidth and exhibits an in-band IM3 of less than −58 dBc. The WBTX consists of a current-steering DAC with digital sinc equalization and roll-off compensation. By implementing high-speed, feed-forward pipelined digital logic, the DAC sampling rate extends to 5 GHz. The WBTX can deliver up to +11 dBm of output power while consuming only 375 mW. The WBTX occupies 1.65 mm^2 of area.**

I. Introduction

The increasing demand for higher data rates in cable applications requires the use of transmitters with signal bandwidths in the gigahertz order with a less than 50 dBc distortion floor. Conventional homodyne transmitters can be considered for the task, but they lack sufficient bandwidth. Recent work reports bandwidths in the order of two hundred MHz (e. g., [1]). Moreover, using multiple conventional TXs in parallel is unattractive due to the prohibitively high power consumption and area required.

A new category of high-speed, high-resolution embedded DACs is enabling WBTXs for high data-rate communication in cable applications.

The presented WBTX (see Fig. 1) consists of a 9-bit 5 GS/s current-steering TXDAC with digital sinc equalization and roll-off compensation, and an external image reject band pass filter. The TXDAC also embeds a high-speed digital interface to serialize the 625 MHz input digital data stream and feed it to its decoder clocked at 5 GHz.

When compared to a conventional homodyne TX, no additional analog circuitry is required to compensate for I/Q imbalance, since complex signal processing is done in the digital domain. Moreover, this WBTX only consumes 375 mW and can deliver up to +11 dBm of output power, thus relinquishing the need for an internal power amplifier driver, relative to [1].

The main challenges in designing the WBTX are achieving the high sampling frequency (f_S) while still maintaining high in-band linearity and low-level spurs.

The paper describes the solutions found to overcome these challenges. Section II focuses on the specially designed high-speed, feed-forward pipelined digital logic that enabled the 5 GS/s TXDAC sampling rate. Section III presents the optimizations on the WBTX decoder that extended the TX signal bandwidth beyond 2 GHz with an in-band IM3of less than −58 dBc, thus obsoleting the classical WBTX (e. g., [1]).

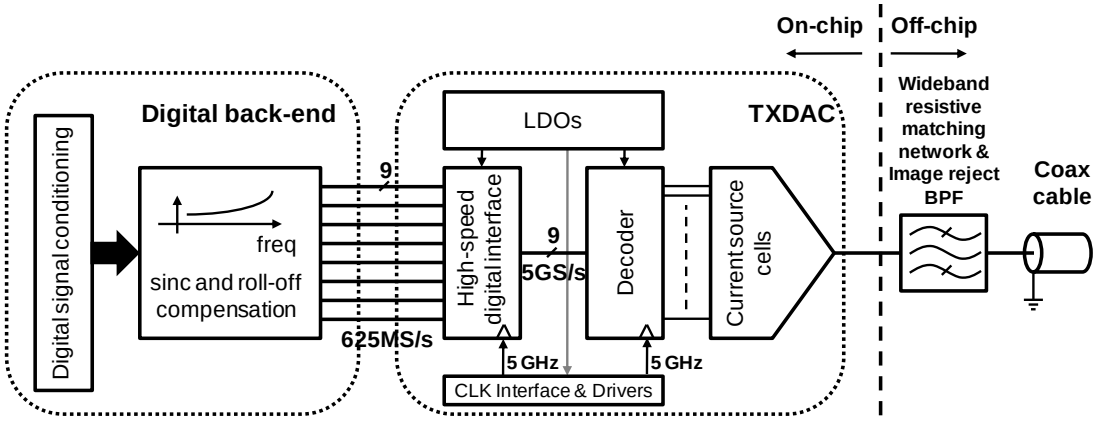

Figure 1. WBTX block diagram.

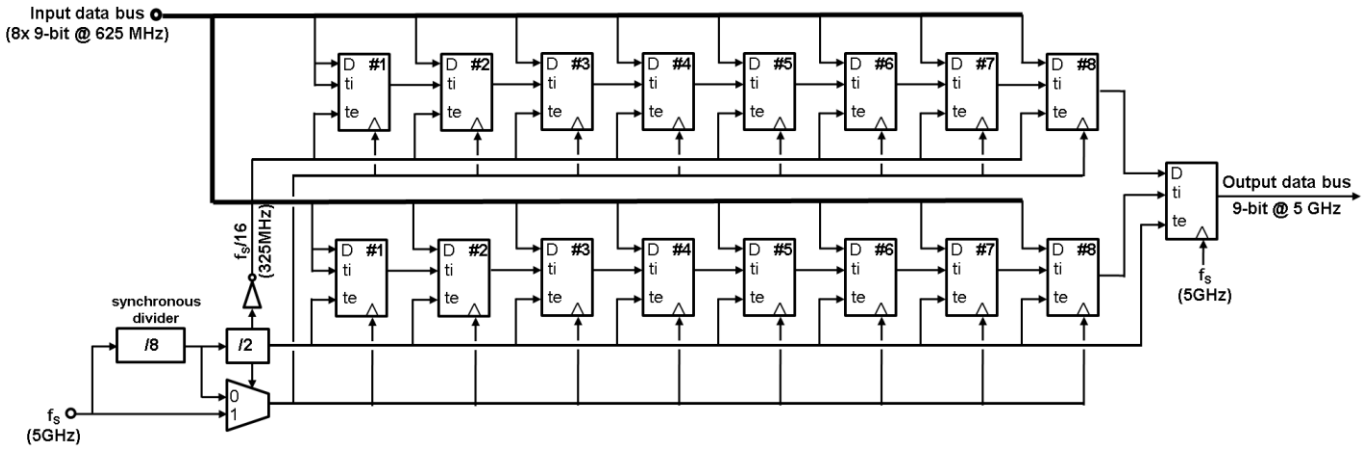

Figure 2. High speed digital interface schematic.

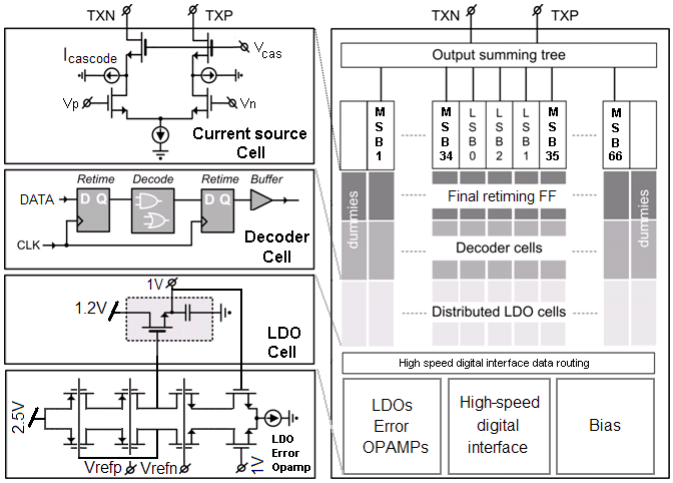

Figure 3. TXDAC simplified floor plan and circuit details.

To conclude the paper, Section IV presents the resulting measurements.

II. High-Speed Digital Interface Design

The digital back-end speed is typically limited to a few hundred megahertz. In this case, it delivers the TX data over *eight* 9-bit channels, each running at $f_S/8$ (i. e., 625 MHz). These low-frequency data streams must be serialized by the digital interface to *one* 9-bit 5 GS/s stream that drives the TX decoder (see Fig. 1).

To solve this bottleneck for high-frequency TX operation, a *feed-forward* 8-to-1 CMOS scan-FF based serializer was developed. The serializer block schematic is depicted in Fig. 2. The scan-FF behaves like a normal D-FF when its "te" input is low. For "te" high, the FF takes its data from the "ti" input instead of the "D" input. Hence, there is no need for any additional glue logic in-between the chain of 9-bit registers from Fig. 2.

The serializer operation is straightforward and does not require a controller or precharging circuits. When the control clock $f_S/16$ is high, the lower bank of registers is shifted to the right at a rate of f_S, while the upper registers are loaded with incoming data at a rate of $f_S/8$. When the $f_S/16$ clock is low, the upper bank of registers is shifted to the right. Thus, the implemented serializer power consumption is only 8 mW and it occupies only 0.0015 mm^2.

III. Optimizing the WBTX Decoder for High TX Sampling Frequency and Linear Response

To avoid non-monotonicity and to reduce glitch energy, the 9-bit TXDAC uses thermometric coding for the first 6 MSBs. Hence, the TXDAC core consists of 66 current source cells (i. e., 63 MSBs and 3 LSBs). The current source cell schematic is shown in the upper left corner of Fig. 3. To improve the high-frequency linearity, the current source cells use the currents $I_{cascode}$ to keep the cascodes always on [2].

Two issues still need to be overcome with respect to achieving (i) the TXDAC high sampling frequency while (ii) maintaining the high TX linearity.

First, there is a potential speed bottleneck at the interface between the decoder and current source cells, given that 66 DAC cells have a total width of almost 1 mm due to the matching requirements of their current sources. To minimize the interconnect length of the decoder outputs and, the associated delay limiting the maximum operating frequency, a distributed decoder is created. Hence, each TXDAC current cell is driven by its own dedicated decoder cell, which consists of the decode logic encapsulated in a pipeline stage as depicted in the Fig. 3. By pipelining the 9-bit distributed decoder input, the 5 GHz sampling frequency is achieved.

Second, there is a requirement for a highly linear TX operation and because of this, special measures need to be taken given its high operation frequency as described later in this paper.

A. Optimal interface to the analog cells

As mentioned, to every analog current source cell, a dedicated corresponding digital decoder cell was created. However, a special cell is required between the two in order to optimally transition from the digital realm to the analog: *the final retiming flip-flop*. The flip-flop comprises two custom made pseudo-differential CMOS latches.

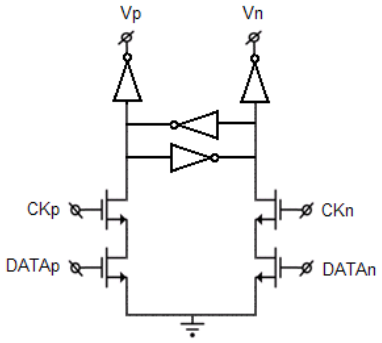

Figure 4. Final latch schematic.

The final latch schematic is depicted in Fig. 4. The CMOS implementation is preferred to the CML, given its lower power consumption and the benefits of having the steepest transition, [2, 3]. By properly sizing the inverters, the optimal differential output signal trip point is found, such that the WBTX linearity is maximized. Moreover, the latch can directly drive the analog current cells and the need of AC coupling capacitors is relinquished, minimizing the overall circuit area.

B. Overcoming the layout and package parasitics

Layout and package parasitics create supply impedances that cause a signal-dependent ripple on the supplies. This reduces the TX linearity by modulating the exact timing moment the current cells switch. Therefore, the TXDAC digital circuits driving the current cells are placed under LDOs embedding high-Q decoupling capacitors on the regulated voltage output. Given the pitch of the TXDAC cells, there is the danger that a voltage drop across the long supply lines creates an additional timing mismatch.

Hence, the solution is found by designing *distributed* LDO cells out of its nMOS pass transistors with local decoupling capacitors (see Fig. 3). Each pass transistor cell is placed as close as possible to the decoder and current cells it is supplying, making the supply connections short and identical for each cell. A side benefit is that the cells are now shielded from other sources of supply noise (e. g., noise generated by the RX and digital back end). A separated sensing wire shorts the output of all of the LDO cells and is fed back to a telescopic error amplifier to close the voltage regulation loop. By splitting the error amplifier and pass transistor supplies as shown in Fig. 3, the LDO power efficiency is increased.

These techniques, together with the 1.2 V LDO pass transistor supply, ensured only 120 mW of power consumption for the digital blocks, including the clock buffers.

IV. Measurement Results

The WBTX has been implemented in a 40 nm CMOS process. Fig. 5 shows the die photo. The chip area is 1.65 mm^2, including the digital circuitry. All measurements are taken at the WBTX output, before the external 6^{th} order Chebyshev low-cost image rejection filter. The sampling clock is set at 4968 MHz.

Fig. 6.a shows the WBTX output spectrum for a 200 MHz tone, confirming the low spur level due to the dedicated pseudo-differential drive and distributed LDO approach. The highest spur is at $f_S/8$ and is smaller than 70 dBc. Fig. 6.b shows the two-tone linearity versus signal frequency with 5 MHz tone spacing. The WBTX is achieving an IM3 of <−58 dBc over a 2.2 GHz bandwidth. Fig. 6.c shows the WBTX output spectrum for a 150 MHz multi-tone signal made out of 23 CW carriers summing a total power of –6 dBm. The measured out-of-band SFDR is larger than 60 dBc. To verify the WBTX bandwidth flatness, a multitone signal of 23 CW spanning over 1.2 GHz, from 0.95 GHz to 2.15 GHz, was applied to the TX. Fig. 6.d shows the WBTX output measured with and without digital sinc and roll-off compensation. The bandwidth flatness is within ±1 dB when digital compensation is enabled.

V. Conclusions

This paper presented a TXDAC-based WBTX for cable applications in 40nm CMOS. Table I summarizes the WBTX performance and compares it with other similar circuits.

The 5 GS/s WBTX sampling rate is achieved by designing dedicated high-speed, feed-forward pipelined digital logic, and distributing the decoder design. By distributing the digital circuit supply voltage regulators, the layout and package parasitics influence is minimized. The transition from the digital input data stream to the analog current cells is optimized by using a pseudo-differential custom designed CMOS latch. Hence, the TX signal bandwidth is extended beyond 2 GHz and an in-band IM3 of less than −58 dBc is achieved, obsoleting the classical homodyne WBTX.

Since complex signal processing is done in the digital domain, no additional analog circuitry is required to compensate for I/Q imbalance. Moreover, while consuming only 375 mW, the WBTX is able to output +11 dBm.

Finally, the measurements in Fig. 6 together with the 375 mW power consumption revealed that the presented WBTX is suited for both narrow and wide-band cable applications.

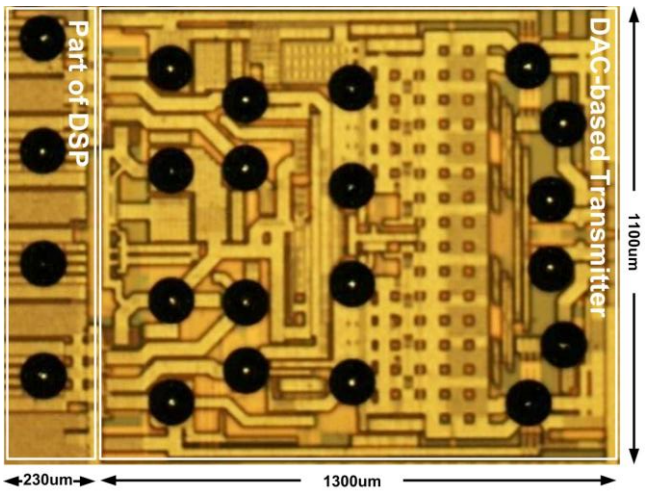

Figure 5. WBTX die photo.

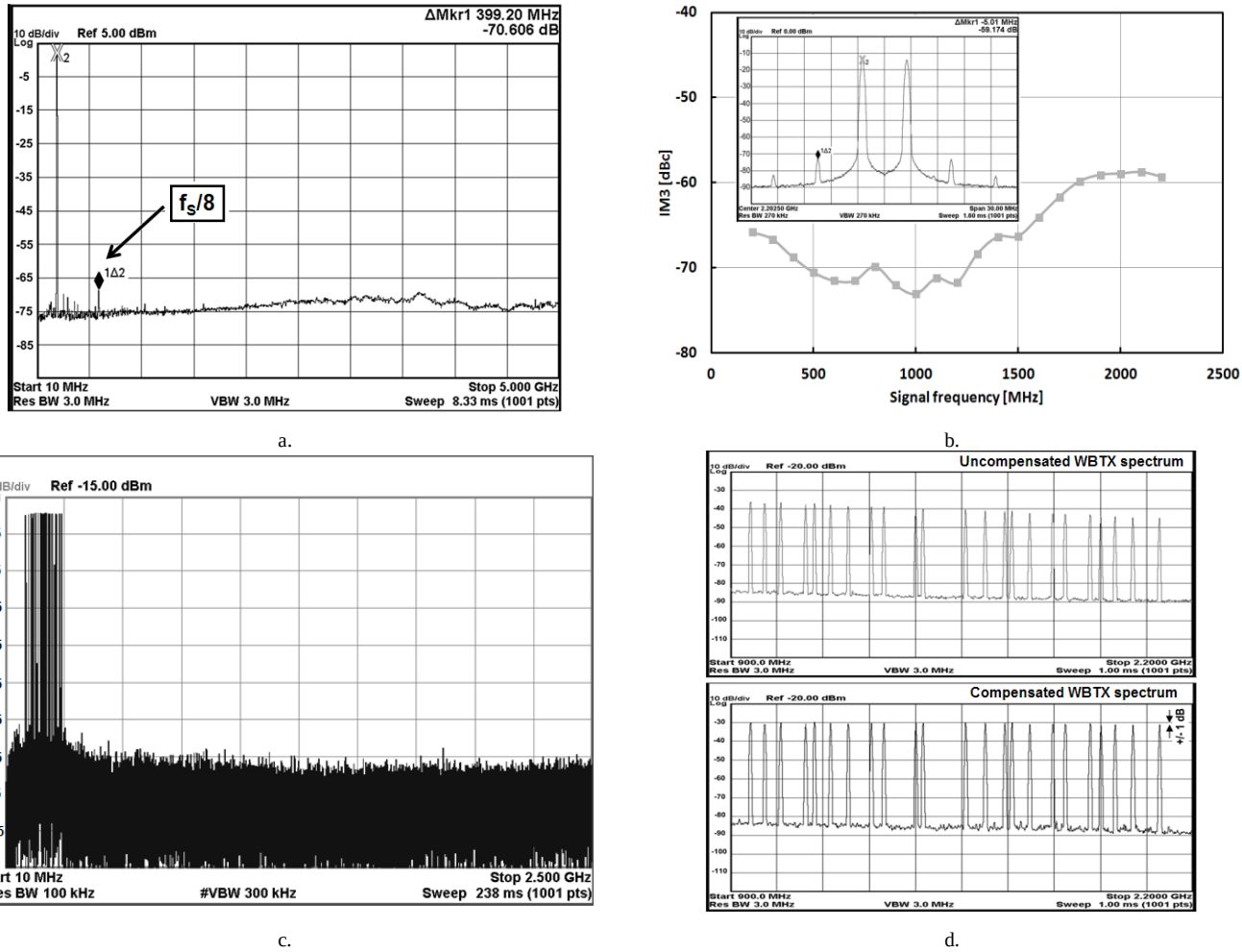

Figure 6. a. WBTX output spectrum for a 200 MHz tone, b. WBTX IM3 vs. frequency, c. WBTX output spectrum for a narrow band multi-carrier signal, d. WBTX output spectrum for a wide-band multi-carrier signal with and without digital sinc and roll-off compensation.

TABLE I. WBTX PERFORMANCE SUMMARY AND COMPARISON WITH SIMILAR WORKS

Parameter	Value		
	This work	**[2]**	**[4]**
Effective signal bandwidth	2.2 GHz	1.2 GHz	0.8 GHz
Sampling frequency	5 GHz	2.9 GHz	1.6 GHz
Maximum output power	+11dBm(75)	+10.2dBm(75)*	–3.5dBm(75)*
IM3	< – 58 dBc up to 2.2 GHz	< – 52 dBc up to 1.2 GHz	< – 62 dBc up to 0.8 GHz
Power consumption	375 mW	188 mW	1200 mW
Process / Area	40nm CMOS 1.65 mm^2	65nm CMOS 0.31 mm^2	GaAs Bipolar 3.24 mm^2

*Normalized to 75Ω.

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