A Surface-Mounted RF IC Technology Demonstrated with a 10 GHz LC Oscillator with Copper Coils

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Abstract

A surface-mounted RF IC fabrication technology is presented that includes a substrate transfer processing step to glass. The fabrication technology uses copper in one of the last fabrication steps to form contacts and inductors. To demonstrate the technology, a differential varactorless 10 GHz LC oscillator is fabricated. The quality factor of the used 0.63nH inductor is estimated by measuring the required start-up current of the oscillator. With a supply voltage of 3V, the estimated quality factor is as high as 39 at 10 GHz. At 10 GHz the dissipation of the oscillator core is 0.42 mW (with 3V supply voltage) and the measured phase noise better than -94.7dBc/Hz at 1 MHz offset of the carrier. By increasing the bias current, the frequency can be tuned from 10.2 GHz to 8.7 GHz, which corresponds to 15.8% tuning range. The proposed fabrication technology eliminates bond-wires, reduces cross-talk and yields excellent passives.

Introduction

New wireless applications put a constant pressure on RF technologies. Sustained effort is directed to improve technology figures of merit (FOMs) like transition frequency (f_T), input and output bandwidth (f_V, f_{OUT}) and unity power gain frequency (f_{MAX}), as well as power consumption and integration level [1, 2]. Examples of new applications are ultra low power transceivers in the ambient intelligent home of the future, that will require high quality passives [3]. Power consumption is also of high importance for portable WLAN transceivers operating at 2.4 GHz, 5.x GHz and 17 GHz. In the future, WLAN applications might well extend to 60 GHz, where a global frequency band is allocated for wireless networks [4]. On top of the low power requirements (and also related to a low power dissipation); packaging of a RF IC technology is an important aspect, especially at 17 GHz and 60 GHz. A bond-wire of only 0.5 mm ($\approx$ 500 pH) already represents an impedance of 16 Ω, 53 Ω and 188 Ω at 5 GHz, 17 GHz and 60 GHz, respectively. Although advanced packing technologies like chip-scale packages reduce package parasitics, surface mounting of the silicon die provides additional performance improvement.

This paper highlights the combination of two fabrication techniques that address the need for low power RF technologies, as well as a way to minimize the negative effects of packaging on RF performance. Specifically, a surface mounted technology (SMT) is described in which a substrate transfer technology to a glass is used. The combination of both fabrication technologies is used for the realization of a 10 GHz LC oscillator. This

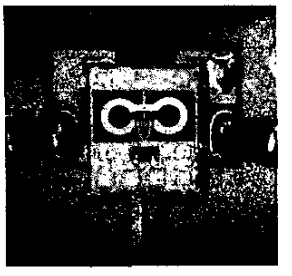

Figure 1. Micro-graph of the surface mounted 10 GHz LC oscillator

demonstrator IC has copper coils that are realized during one process step of the surface mounted fabrication process, yielding very high quality factors. Obviously, other RF building blocks will greatly benefit from the presented fabrication techniques. For example, device and assembly parasitics greatly affect the performance of power amplifiers, and these parasitics can be significantly reduced by the proposed technology [5].

Section 2 describes the surface mounted technology. Next, the design of the LC oscillator is highlighted in section 3, followed by measurements of this oscillator in section 4. The performance of the oscillator is compared against the state of the art in section 5. Finally, some conclusions are made in section 6.

Surface mounted RF IC technology

Substrate Transfer Technology (STT) combines the advantages and performance of main stream silicon processing with a complete freedom on the choice of the substrate [5]. STT is based on gluing a processed silicon wafer, upside down, to an alternative substrate followed by a partial or complete removal of

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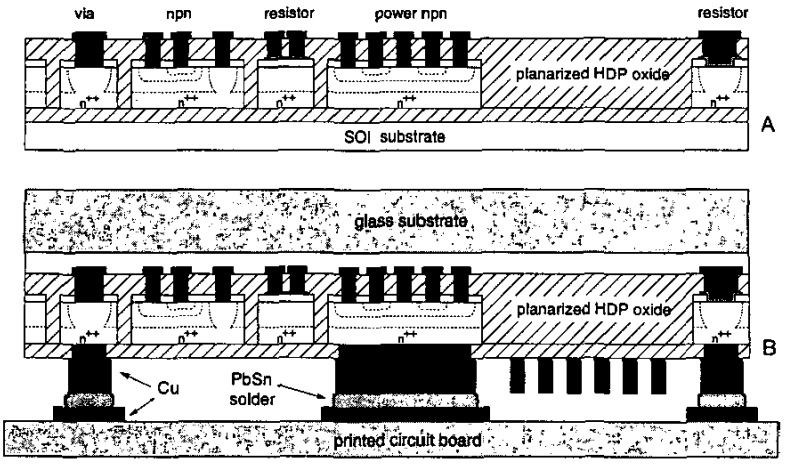

Figure 2. Illustration of the surface mounted RF IC technology.

the original substrate. The alternative substrate is usually glass as it is low cost and has excellent RF properties. The benefits of an excellent insulator as a substrate are threefold:

- *Better passive device are obtained.* For example, quality factors of inductors are greatly improved since substrate losses are minimized. In addition, parasitics of other passive devices (resistors, capacitors) are reduced as well.
- *Cross-talk is reduced.* Capacitive paths between circuits on one die are greatly reduced. This leads to shorter design cycles as the prediction of cross-talk is still cumbersome and strongly dependent on IC technology.
- *Power consumption is reduced.* Interconnect to substrate capacitance, collector/drain to substrate capacitance and others are minimized.

Substrate transfer can be combined with an SMT that tackles package parasitics. The proposed technology is based on a combination of (thick-film) SOI substrates, a standard or slightly modified front-end technology (CMOS, BICMOS or bipolar), followed by a substrate transfer to glass and, finally, surface mounted assembly. The proposed surface mounted RF IC fabrication technology is illustrated by Figure 2, using a bipolar front-end as an example.

SOI substrates with 0.2μm top silicon and 0.4μm thick buried oxide are used as starting material. The top silicon is doped n^{++} to 10^{20} cm^{-3} by diffusion from an arsenic doped glass to form a blanket buried layer. After epi growth, a bipolar front-end (see Figure 2(A)) is fabricated based on a 25 GHz double poly-silicon technology [6]. Normally device isolation is performed before the last high temperature step (RTA emitter anneal), but unconventionally in this case it is done after the RTA step. This is realized by etching trenches down to the buried oxide, High Density Plasma (HDP) oxide filling and Chemical Mechanical Polishing (CMP). By designing the trenches sufficiently far away from any p-type diffusions, junction leakage along trenches is avoided.

Figure 2(A) shows a schematic cross-section of the finished wafer. The back-end trench procedure makes it possible to remove all the silicon in the areas reserved for inductors, filling it with oxide and at the same time retaining a fully planar surface. After transfer to glass, the wafers are flipped and processing continues on the former buried oxide layer. First the oxide is wet etched at the locations where a contact to the backside of the devices is needed (e.g. vias). Next 10μm thick copper patterns are platted to form contacts and inductors. After dicing, the front-end is ready for surface mounting by reflow soldering as show in Figure 2(B). The backside contacted devices allow for an efficient heat removal in the case of RF power devices and minimal series resistance in the case of large decoupling capacitors.

The highlighted SMT in this section is used to realized a 10 GHz LC oscillator as technology demonstrator. Its design and measurement results are discussed in the following two sections, respectively.

A 10 GHz LC oscillator design

The circuit diagram of the LC oscillator is shown in Figure 3. At design time only rough estimates of the device parameters for both active (25 GHz f_T double poly technology) and passive devices in the discussed SMT were available. Therefore, a robust simple cross-coupled pair was chosen to implement the active oscillator pair. Although bipolar transistors (using the emitter-base junction or the collector-base junction) could have been used to realize a varactor, the resonator has been implemented varactorless. Hence, in absence of lumped capacitance, the resonator of the LC oscillator is formed by the 0.63nH coils and parasitic capacitance of the active devices and

the inter-connect. This allows estimation of the inductor quality factor at 10 GHz by measuring the start-up current, as will be discussed below.

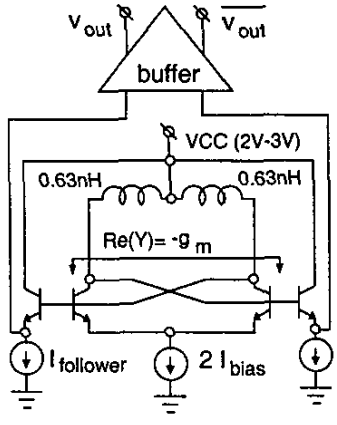

Figure 3. Circuit diagram of the varactorless 10 GHz technology demonstrator: a LC oscillator, with a 50Ω output buffer.

The output buffer in Figure 3 consists of emitter followers, followed by a differential stage with 50Ω collector resistors. This limiting buffer is designed (excluding insertion loss in measurement cables and connectors) to deliver -20 dBm at the 50Ω input of a spectrum analyzer.

Experimental results

Figure 4 shows the surface mounted LC oscillator. The active oscillator part has been enlarged and photographed with backside illumination, and is shown below the photo of the oscillator die with PCB. A fine grid of trenches is used in the region of the active circuitry, for a maximum reduction of inter-connect and inter-device capacitances.

VCC	$I_{bias} = 100\mu A$	$I_{bias} = 2mA$
3 V	39 mW	60 mW
2 V	12.7 mW	25.6 mW

Table 1. Measured power dissipation of the oscillator core plus output buffer.

The power dissipation of the chip for several combinations of current I_{bias} and VCC is given in Table 1. As indicated in Figure 3, the tail current of the active oscillator part is $2I_{bias}$. The buffer dissipation, with on-chip biasing network, substantially increases when VCC is increased and dominates the total power dissipation. For example, for VCC=3V and $I_{bias} = 70\mu A$, the LC oscillator core dissipates only 0.42 mW. Table 2 shows the measured I_{bias} current for which the oscillator starts-up for two VCC values. In other words, it shows for which tail current $(2 \cdot I_{bias})$ the gain condition for oscillation is

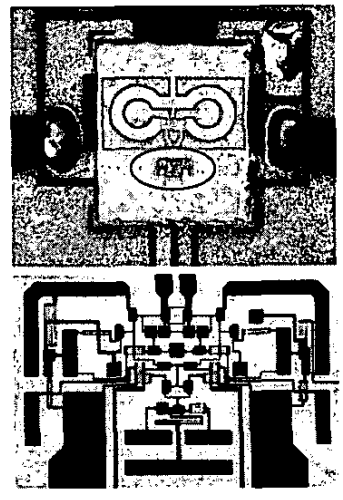

Figure 4. Die photo and detailed view of the active part of the surface mounted 10 GHz LC oscillator.

fulfilled. Using this current value for biasing, the transconductance (g_m, see Figure 3) of the active oscillator part is simulated at 10 GHz. The effective parallel resonator resistance is equal to $-1/g_m$. With this parameter a first order estimation of the quality factor of the 0.63nH inductor can be derived:

$$Q_{l'} \approx \frac{-1/g_{m_{start-up}}}{2\pi \cdot 10\,\text{GHz} \cdot 2 \cdot 0.63\,\text{nH}} \qquad (1)$$

Since g_m is defined differentially, two times 0.63 nH is used in (1). For VCC equal to 3V and 2 V the estimated Q is 39 and 25, respectively.

VCC	meas. start-up I_{bias}	sim. start-up g_m@10 GHz	$Q_{l'}$ @10GHz
3 V	9.7 μA	-318 μS	39
2 V	37.5 μA	-492 μS	25

Table 2. Estimated inductor quality factor at 10 GHz.

A lower Q value for a supply voltage of 2 V can be expected since the junction capacitances in the bipolar active oscillator part are larger for this voltage, and represent (e.g. by their parasitic series resistance) more losses at 10 GHz. The Q values in Table 2 make clear that excellent Q factors are achievable at 10 GHz, when the discussed surface mounted fabrication technology is used with its copper back-end processing step.
Although the oscillator has a varactorless resonator, a significant tuning range can be achieved by varying the base-emitter diffusion capacitance, which value is a function of I_{bias}. For a practical application, varactors are preferable since we now

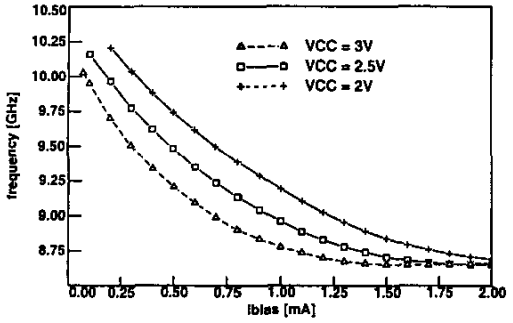

Figure 5. Oscillation frequency versus I_{bias} for VCC is 2V, 2.5V and 3V.

use a parasitic effect to tune, and the carrier amplitude variation (and thus the phase noise to carrier level $\mathcal{L}(f_m)$) and tuning range are directly coupled, making oscillator optimization more difficult. Nonetheless, a significant tuning range can be obtained with I_{bias} as shown in Figure 5. For VCC equals 3V, the tuning range is slightly lower compared to 2V, because the buffer then has a higher biasing level (see Table 1), and is loading the oscillator core more.

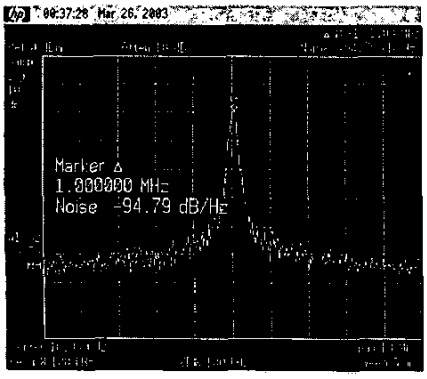

Figure 6. The power spectrum of the oscillator at 10 GHz (VCC=3V and I_{bias}=70 μm).

Figure 6 shows the power spectrum of the LC oscillator close to the maximum frequency at 10 GHz and with 3V supply voltage. The observed $\mathcal{L}(1\,\text{MHz})$, verified by repeated measurements, is better than -94 dBc/Hz. With a supply voltage of 2V and a slightly higher I_{bias} (120 μm), $\mathcal{L}(1\,\text{MHz})$ is about -95 dBc/Hz at 10.2 GHz.

Benchmarking

Table 3 compares the performance of this work, with the phase noise normalized for power, frequency and offset frequency f_m [1], with three other designs. With the lowest power dissipation in absolute sense, an excellent $\mathcal{L}_{norm}(f_m)$ is obtained. Note that phase noise measurements are performed with standard power supplies, and a battery-operated oscillator is expected to be more stable, due to a minimum amount of external noise that modulates the oscillator.

Ref.	freq. (GHz)	P_{diss} (mW)	$\mathcal{L}_{norm}(f_m)$ (dBc/Hz)
This work	10	0.42	-178
[7]	11	24	-173
[8]	13	39	-159
[9]	17	10.5	-182

Table 3. Benchmarking of several published LC oscillator running at 10 GHz and higher.

Conclusions

Surface mounted technology is an important enabler to achieve better performance of passives at high frequencies, to significantly reduce package parasitics, to eliminate bond-wires and to reduce cross-talk. These advantages translate into ultra low-power circuits. The surface mounted RF IC technology discussed in this paper uses copper to form the contacts as well as high-Q inductors. The achieved (loaded) quality factor at 10 GHz was estimated at 39. A 10 GHz LC oscillator has been integrated in a 25 GHz f_T surface mounted double poly technology. It dissipates 0.42mW at 10 GHz and has a $\mathcal{L}(1\,\text{MHz})$ better than -94 dBc/Hz, with 3V supply voltage.

Acknowledgment

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