A Monolithic 0.4 mW SOA LC Voltage-Controlled Oscillator

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Abstract

A fully integrated LC voltage-controlled oscillator (VCO) design is presented with a VCO core dissipation of only 0.4 mW. Silicon on Anything technology (SOA) is used for implementation. The device library of SOA consist of high quality coils, varactors and low power transistors. With these key components, SOA enables VCO design for high tuning range and low phase noise at very low current levels. Measured VCO tuning range starts at 668 MHz and extends to 830 MHz which corresponds to 21.6% tuning range. Within this tuning range, the carrier to noise ratio (CNR) at 100 kHz offset frequency varies from 98.1 to 100.4 dBc/Hz. Comparison of this work with 8 recently published monolithic LC oscillators, establishes state of the art performance concerning power dissipation, tuning range and carrier to noise ratio.

1. Introduction

High quality (Q) inductors and varactors are required components for monolithic low power and low noise tunable oscillators. Low power is essential in wireless systems such as mobile phones since it directly influences selling features like standby and talk time. Ohmic losses, skin-effect and substrate-losses decrease the Q factor of integrated coils. Parasitic capacitance decreases the self-resonance of the coils but also the available tuning range of integrated varactors. A fundamental improvement towards low power is achieved with the bipolar SOA process, in which the complete silicon substrate is removed and replaced by an insulator, e.g. glass [1]. Also the lateral transistor structure which yields a f_t of 9.2 GHz at a collector current of 63 μA contributes to low power designs [1].

In order to demonstrate the low power properties of SOA technology, a monolithic LC oscillator has been designed using the high Q coils and varactors of SOA's device library. The varactor is constructed with seven parallel sections which each can be removed by laser-cutting. This allows centering of the oscillation frequency to suite a specific receiver/transceiver application. In the presented work all seven varactor sections are operative, resulting in a tuning range of 21.6% with center frequency of 749 MHz. Using the figure of merit defined in [1, 2], which normalizes for frequency and power, -182.7 dBc/Hz is achieved. This is the highest figure of merit reported for monolithic VCOs. Benchmarking of the presented design regarding power dissipation also establishes state of the art performance.

2. Silicon on Anything

The SOA technology combines low power active devices with high Q passives. The on-chip inductors show Q-factors up to 60 @ 2.7 GHz for 1.2 nH inductance. Therefore SOA is well suited for integrated front-ends including all RF filters. Varactors for tuning and compensation of the process spread with sufficiently high Q-factors (33 @ 1.9 GHz) are also available. The 13 masks and the 1 μm lithography keep the process costs low enough, so that even complex filters can be integrated economically.

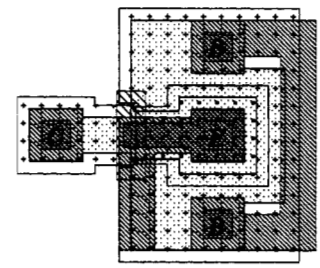

Figure 1. Layout of the NPN.

The low power consumption is achieved by entirely embedding the transistors in insulators. In case of the NPN, the intrinsic part of the vertical structure has been cut out and put in parallel to the wafer's surface. This results in a structure with a lateral current flow and with the normal doping concentrations (figure 1). In the vertically oriented emitter area one dimension is defined by the epi-layer thickness (0.2 μm). This allows emitter-base (and collector-base) junctions of 0.2 μm^2, resulting in very small junction capacitances (0.8 fF and 0.22 fF respectively).

The PNP is a standard lateral transistor also with a minimum emitter area of 0.2 μm^2 (junction capacitances of 0.22 fF). In order to obtain these minimal parasitics, the silicon substrate has to be removed and replaced by a glass substrate. As a result the transistor output bandwidth f_{out} is much closer to transition frequency f_t compared to silicon bulk processes. Furthermore, the mentioned Q-factors of the inductors can only be obtained by removal of the silicon substrate. The maximum supply voltage of the pro-

cess goes up to 12 Volt and can be determined by the width of the collector drift region, which is a geometry parameter in the transistors. The process also offers a bipolar I^2L logic running down to 0.7 Volt, having a normalized gate density of 5000 gates/mm^2 and a gate delay of down to 2 ns. A digital design flow environment is available to support mixed-signal design.

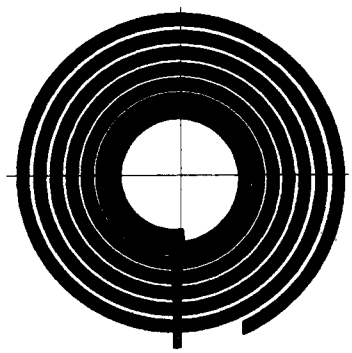

Figure 2. Layout of the optimized inductor.

Figure 2 shows the layout of the inductor used in the VCO design. The distance between the curls is increased with a square root law in order to tune each curl to approximately the same frequency. Note that this scaling depends on the initial distance d_0 between the inner curls and the inner radius R_0. The bridge also deviates from a constant width; the outer crossings are smaller in order to shift the poles – formed of the inductance of all inner curls and the crossing capacitance – together. For larger inductors (higher number of turns) this compensation becomes less effective. Hence the impact of these measures on the Q-factor is between 5% and 12% depending on the inductor's geometry parameters. Measured Q-factors of three inductors are shown in figure 3.

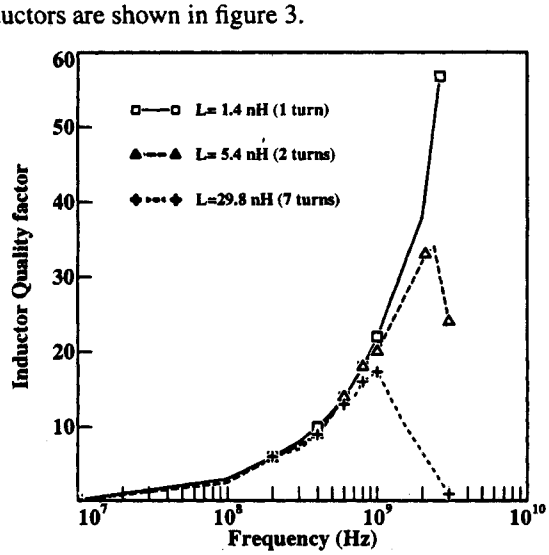

Figure 3. Q-factor measurement results of three inductors.

A single varactor structure is shown in figure 4. It is build up similar to the emitter-base complex of the NPN

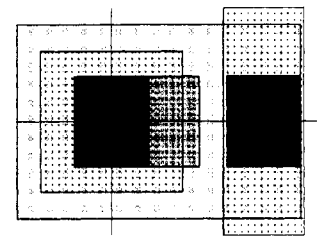

Figure 4. Layout of the used varactor.

transistor and allows to exchange Q versus C_{max}/C_{min} by design parameters. These basic cells are put together by a varactor layout generator in order to build up larger arrays. In narrow band systems the mentioned maximum Q-factors can be obtained. In the varactor-cell used in the VCO the length of the low doped (drift) region is 1.2 μm. After realization of the VCO design new layout design rules currently allow a minimum drift-region of 0.8 μm. This results in higher Q-factors as can be seen in figure 5.

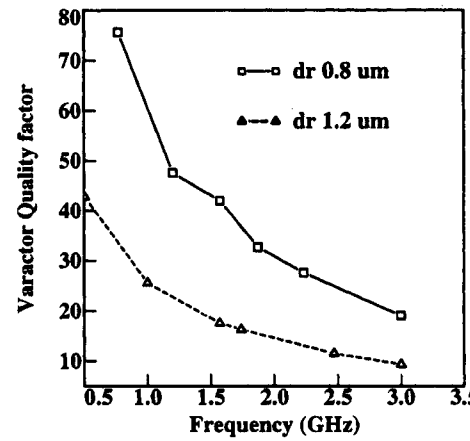

Figure 5. Q-factor measurement results of two varactors with drift regions (dr) 0.8 and 1.2 μm.

3. Balanced oscillator design

A balanced oscillator topology was chosen for the design to maximize rejection of common mode disturbances. It is shown in figure 6. Common mode rejection is especially important in case of integration of the VCO together with other sub-systems, such as in a full receiver/transceiver system. The disadvantage of a balanced LC oscillator design with integrated coils is a substantial increase of chip area, since the inductor area dominates.

The value of the on-chip inductors is 29.8 nH with a Q_{max} of ~ 17.3 at 1 GHz (figure 3). Total parasitic capacitance of this coil is 150 fF. Seven varactor sections in parallel of each 240 fF (zero bias) are used. C_{max}/C_{min} for bias voltage $V_{reverse}$ ranging from 0 to 5 Volt, is approximately 1.7. The quality factor of the varactor is around 26 at 1 GHz (see figure 5 with dr is 1.2 μm). Total current consumption of the VCO consists of twice I_{em} (40 μA) plus I_{vco} (80 μA). Nominal supply voltage was 5

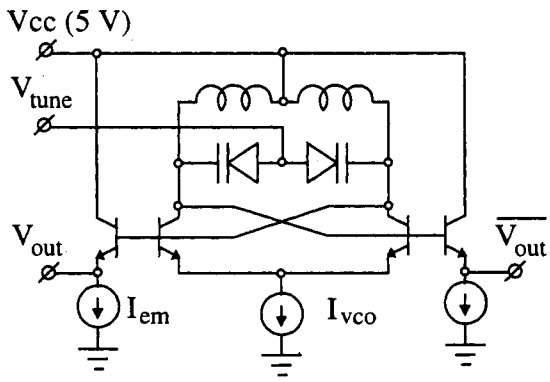

Figure 6. Simplified schematic of the oscillator.

Volt to demonstrate maximum tuning range. Dissipation of the VCO can be lowered by lowering Vcc at the cost of a slightly reduced tuning range.

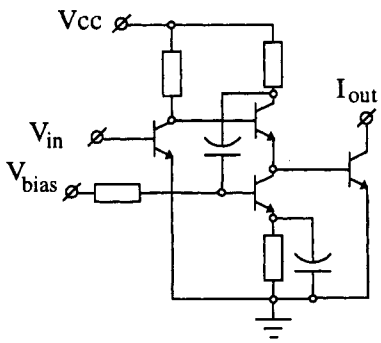

Figure 7. Half circuit of the output buffer.

In cascade with the VCO plus emitter followers, an open collector output buffer is implemented which delivers -30 dBm in 50 Ω. The schematic of the half circuit of the differential buffer is shown in figure 7. Without special measures in the output buffer a multi-oscillation occurred [10]. During a multi-oscillation, two or more simultaneous oscillations exist in steady state. In case of the VCO design, one of the two simultaneous oscillations was introduced by the loading of the buffer. This resulted in a severely distorted VCO output signal. The feedback in the second stage of the buffer reduces the loading on the VCO circuitry substantially and eliminates the multi-oscillation phenomena. Total dissipation of the output buffer is 7.2 mW.

4. Experimental results

A die photo of the monolithic LC oscillator is shown in figure 8. The two inductors occupy a dominant part of the 1940 μm × 1280 μm active chip area. On the left the output buffer can be seen together with a second identical buffer for stand alone characterization. Frequency and carrier to noise (CNR) measurements are performed with a HP8562E spectrum analyzer with pre-amplifier. Frequency versus tuning voltage V_{tune} measurements are presented in figure 9. Measured tuning range is 668 MHz to

Figure 8. Die photo of the LC oscillator.

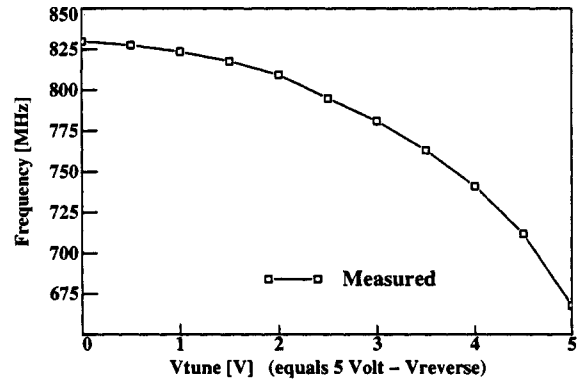

Figure 9. Frequency versus V_{tune}.

830 MHz when V_{tune} is varied from 5 to 0 Volt. Phase noise measurements are shown in figure 10. For the tuning voltage range from 5 to 0 Volt, CNR(100 kHz) varies between 98.1 and 100.4 dBc/Hz.

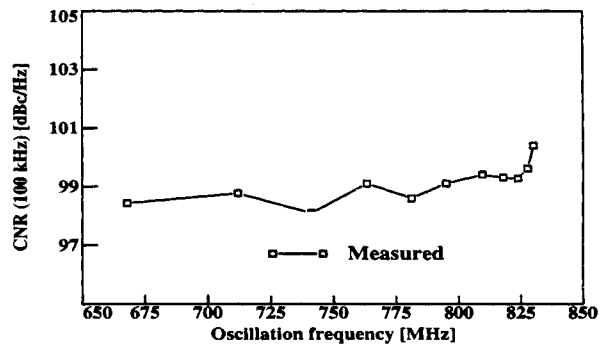

Figure 10. CNR (100 kHz) versus frequency.

The power spectrum of the oscillator with V_{tune} is 0 Volt is shown in figure 11.

5. Benchmarking

In order to benchmark the dissipation of the realized SOA oscillator, figure 12 compares the power dissipation of *this work* with 8 recent publications. With a VCO core dissipation of 0.4 mW ($I_{vco} \times 5 Volt$), the low power properties of SOA are clearly demonstrated.

A comparison of the achieved CNR is based on the fig-

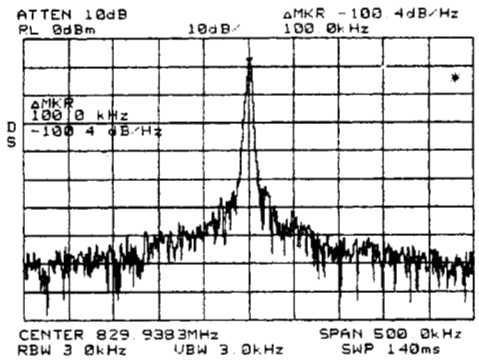

Figure 11. Power spectrum of the SOA oscillator.

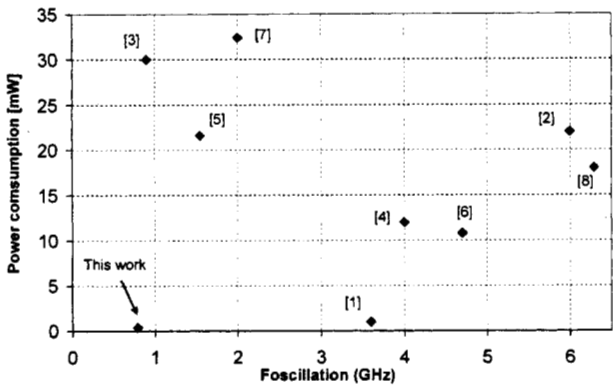

Figure 12. VCO dissipation benchmarking.

ure of merit (FOM) in equation 1 which is used in [1, 2].

$$FOM = -CNR + 10\log\left[\left(\frac{f_m}{f_o}\right)^2 \frac{P_{DC}}{1mW}\right] \quad (1)$$

This FOM normalizes power dissipation of all oscillators to 1 mW and normalizes for offset frequency f_m and oscillation frequency f_o. In figure 13 the FOM of recent publications versus the VCO tuning range is shown. Using the measured CNR value of 100.4 dBc/Hz at 100 kHz of the 830 MHz carrier and 0.4 mW dissipation, this FOM calculates to -182.7 dBc/Hz. This is the highest figure of merit reported for monolithic VCOs.

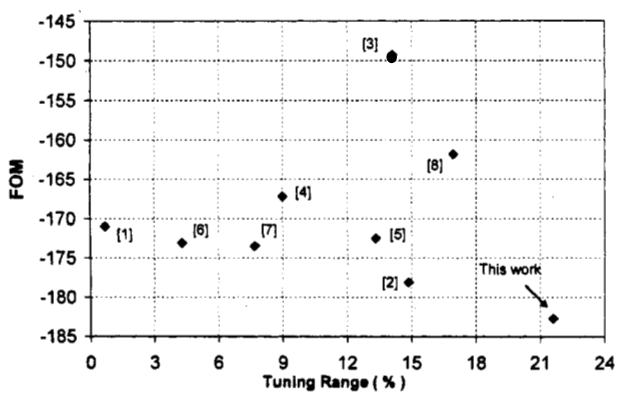

Figure 13. VCO CNR benchmarking.

6. Conclusions

A low power monolithic LC oscillator is realized using SOA technology. State of the art dissipation, CNR and tuning range are demonstrated. The tuning characteristic of the VCO starts at 668 MHz and extends to 830 MHz, thus achieving 21.6% tuning range. Using only 0.4 mW for the VCO core, carrier to noise ratios ranging from 98.1 to 100.4 dBc/Hz at 100 kHz offset are achieved. Benchmarking of this work with 8 recently published monolithic LC oscillators, establishes state of the art performance regarding power dissipation, tuning range and carrier to noise ratio.

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