A HIGH GAIN, LOW VOLTAGE FOLDED-SWITCHING MIXER WITH CURRENT-REUSE IN 0.18 μm CMOS

Vojkan Vidojkovic, Johan van der Tang, Arjan Leeuwenburgh† and Arthur van Roermund

Eindhoven University of Technology, Mixed-signal Microelectronics (MsM) group
Den Dolech 2, P.O. Box 513, 5600 MB Eindhoven, The Netherlands
† National Semiconductor, Het Zuiderkruis 53, 5215 MV, 's-Hertogenbosch, The Netherlands
v.vidojkovic@tue.nl

Abstract **The scaling of the CMOS technologies has a great impact on analog design. The most severe consequence is a reduction of the voltage supply. In this article, a new low voltage folded-switching mixer with current reuse, which operates at 1 V supply voltage, is discussed. The main advantages of the introduced mixer topology are: a high voltage gain, a moderate noise figure and an operation at low supply voltages. Full insight into mixer operation is given by analyzing voltage gain, noise figure, linearity (*IIP*3) and DC stability. The mixer is designed and implemented in 0.18 μm CMOS technology with MIM capacitors as an option. The active chip area is 160 μm $\times$ 200 μm. At 2.4 GHz a single side band (SSB) noise figure of** 13.9 dB, **a voltage gain of** 11.9 dB **and** *IIP*3 **of** -3 dBm **are measured at a supply voltage of** 1 V **and with a power consumption of** 3.2 mW.

I. INTRODUCTION

CMOS technology scaling, migrating towards deep submicron processes, yields a constant improvement in power consumption, speed and number of transistors per unit area. The idea to avoid the need for an analog front-end by connecting analog to digital converter (ADC) immediately to the antenna is not yet feasible. The performance of todays analog to digital converters are the bottleneck. They are still far away from the required ones for such a purpose. Taking into account that fact and driven by the requirements to reduce the cost by implementing the analog and digital part of RF transceivers in the same technology and on the same chip, RF analog designers have to find solutions for RF analog circuits in new submicron CMOS technologies. While CMOS technology scaling is quite beneficial for digital circuits, it is not the case for RF analog circuits and the redesign of RF analog circuits in a new CMOS technology is rather difficult. The most severe consequence of the technology scaling, that affects RF analog designers, is a reduction of the voltage supply. Insufficient voltage room can cause that some circuit topologies can not satisfy the required specifications or even they can not operate. Hence, research into low-voltage circuit topologies is important.

This paper, discusses a low voltage mixer that can have a 1 V supply voltage and still offers good performance. The first step to arrive at a suitable mixer topology, is to select an appropriate way to realize the mixing operation in CMOS technology. This selection has been done between three possibilities. The first one is to use a MOS transistor in the linear region. In this way, a passive linear mixer is obtained [1]. This mixer has a very high linearity (*IIP*3 around 40 dBm) but its *NF* is very high (around 30 dB). Such a *NF* will lower the sensitivity of a receiver front-end too much. The second possibility is to exploit the square law characteristic of a MOS transistor [2]. The disadvantage of this mixer is a low gain (around 2 dB). The third possibility is to realize a switching mixer. A well known example is the Gilbert-cell mixer. The overall performance of the Gilbert cell mixer is normally sufficient for a majority of applications (*NF* around 10 dB, gain around 10 dB and *IIP*3 around 1 dBm at power dissipation levels around 6 mW) [7], but it can not stand very well low supply voltages. The reduction of the supply voltage will cause severe limitations in the mixer performance because, three transistors are stacked. The proposed folded-switching mixer with current-reuse can be regarded as a modification of the Gilbert-cell mixer, that can allow a low voltage operation.

II. BASIC OPERATION

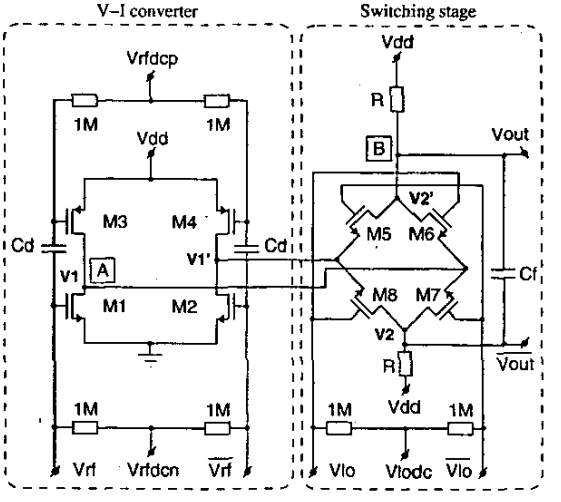

Figure 1. Folded-switching mixer with current-reuse

The folded-switching mixer with current-reuse is depicted in Fig. 1. In the presented mixer topology the stage that represents the

0-7803-8333-8/04/$20.00 © 2004 IEEE

voltage to current (V-I) converter and the switching stage are connected in a way such that the switching transistors are folded with respect to the transistors in the V-I converter. This novel connection method yields low-voltage operation. The major part of the DC current in the mixer flows through the transistors in the V-I converter and only a small amount of the DC current flows through the switching transistors, yielding low voltage drop across the load resistors. In this way the problems that appear in the case of the Gilbert cell mixer are avoided and the folded-switching mixer can be designed to operate at low supply voltages (down to 1 V). The current reuse principle is for the first time introduced in [6]. This is an efficient way to have a high voltage gain and a low noise figure with a low power dissipation.

III. GAIN, NOISE FIGURE AND LINEARITY

The voltage gain of the mixer can be approximated by:

$$G = 20\log(\frac{2}{\pi}(g_{mn}+g_{mp})R) \quad (1)$$

where g_{mn} is the transconductance of M1 and M2 and g_{mp} is the transconductance of M3 and M4. From (1), it can be seen that transistors M3 and M4 both contribute to the voltage gain, which is the result of the applied current reuse principle. Since, the major part of the DC current in the mixer flows through the transistors in the V-I converter and only a small amount of the DC current flows through the switching transistors, it is possible to use large load resistors and to obtain a high voltage gain because the voltage drop on the load resistors is low. The DC current through switching transistors can be controlled by V_{lodc} voltage. In this way, voltage V_2 can be kept high allowing a high output voltage swing, that will not corrupt the operation of switching transistors (they should stay in saturation when they conduct). By adjusting the W/L ratio of the transistors M1, M2, M3, M4 and choosing a proper V_{rfdc} voltage, the required transconductance of the V-I converter can be obtained. Voltage V_1 should be sufficiently low in order to provide enough voltage room for the switching transistors to withstand a high output voltage swing that results from a high gain. On the other hand, voltage V_1 should be sufficiently high in order to keep M_1 and M_2 in saturation when an input voltage is applied.

The NF of the folded switching mixer with current reuse can be approximated by:

$$NF = 10\log(2+\frac{4(\gamma_n g_{mn}+\gamma_p g_{mp})}{R_s(g_{mn}+g_{mp})^2}+\frac{\pi^2}{2(g_{mn}+g_{mp})^2 R R_s}) \quad (2)$$

where R_s is the source resistance. Choosing the right biasing voltages V_{rfdcn}, V_{rfdcp} and W/L ratio of the transistors M1, M2, M3 and M4 , sufficiently high transconductance g_{mn} and g_{mp} can be obtained resulting in a low NF.

The transfer function of the mixer (V_{outdif}/V_{indif}) is represented in Fig. 2. At the points A and B the switching transistors are turned off by the high voltage on the node $V1$ or node $V1'$. This can happen when voltage V_{rf} or $\overline{V_{rf}}$ is low. In that case the high current pushed by the transistors M3 or M4 will make a high voltage on the output impedance of the transistors M1 or M2 that will turn off the switching transistors M7 and M6 or M5 and M8. The bumps on the transfer function are caused by the operation of switching transistors in linear region. Linearity depends on L. It can be improved by increasing L and reducing the bumps. In the folded-switching mixer with current-reuse, L can be increased by decreasing the voltage $V1$ and the bumps can be reduced by keeping the switching transistors far from the linear region.

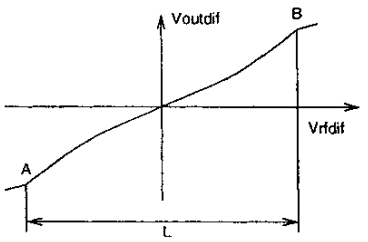

Figure 2. Transfer function of the folded-switching mixer with current-reuse

IV. DC STABILITY

In order to design a robust folded-switching mixer with current-reuse, that can stand the voltage supply variations of 10 %, it is necessary to calculate the variations of voltage V_1 or V_1' as a function of the supply voltage variations (ΔV_{rfdcn} and ΔV_{rfdcp}). This can be done applying the large signal analysis and the Kirchoff's law on the node A (see Fig. 1):

$$I_n = I_p + 2I_s \quad (3)$$

where I_n is the current through the transistor $M1$, I_p through $M3$ and I_s through $M6$ and $M7$. Current I_n can be expressed as:

$$I_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_t)^2(1+\lambda V_1) \quad (4)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length, V_t is the threshold voltage, V_{gs} is the gate-source voltage and λ is channel-length modulation coefficient. Similar equations can be written for currents I_p and I_s. Substituting the expressions for I_n, I_p and I_s in (3), an equation that contains V_1 to the third power is obtained and it is very difficult to solve it in the closed form.

In order to overcome this difficulty, a small signal analysis will be applied assuming that the variations of voltages V_{rfdcn} and V_{rfdcp} are small. This analysis will still give good estimation about the variations of voltage V_1. Substituting the small signal model for each transistor (parallel connection of transistor output impedance and ideal current source with value $g_m V_{in}$, where g_m is the transconductance and V_{in} small signal voltage at the gate) and applying the Kirchoff's law for nodes A and B the variations of voltage $V1$ or $V1'$ can be calculated:

$$\Delta V1 = -\frac{g_{mp}\Delta V_{rfdcp}+g_{mn}\Delta V_{rfdcn}}{1/R_{op}+1/R_{on}+2g_{ms}} \quad (5)$$

where R_{op} and R_{on} are output impedances of transistors $M1$ and $M3$. g_{ms} is the transconductance of the switching transistors. In the denominator g_{ms} (in the design $g_{ms} = 2.5$ mS) dominates and reduces the variations of the voltage $V1$. Taking into account process spread, supply voltage variations of 10 % and temperature variations ($-25°C$ to $70°C$) the worst variations of V_1 are: from 232 mV to 450 mV and nominally $V_1 = 310$ mV. These variations do not deteriorate the circuit operation and there is no need for common mode feedback, which is another advantage of the proposed mixer.

V. EXPERIMENTAL RESULTS

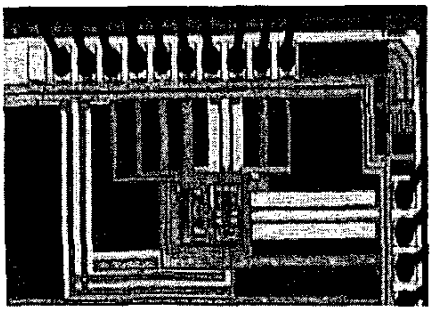

Figure 3. Die micrograph of the folded-switching mixer with current-reuse

Fig.3 shows the micrograph of the realized folded-switching mixer with current-reuse. The active chip area is 160 μm $\times$ 200 μm. Total dissipation of the IC is 8.1 mW at a supply voltage (V_{dd}) of 1.8 V and 3.2 mW at a supply voltage of 1 V.

Fig. 4 shows a measured mixer voltage gain (G) as a function of the differential local oscillator (LO) voltage swing ($V_{lo,dif}$). In Fig. 4 the numbers on the x-axis denote the peak values of the applied differential LO voltage swing. The LO frequency is set to 2.4 GHz, while the output signal is measured at an intermediate frequency (IF) of 1 MHz. As it can be seen, the voltage gain reaches the highest value for $V_{lo,dif}$ = 500 mV. For $V_{lo,dif}$ lower than 500 mV_p, the voltage gain is reduced because such a LO voltage swing is not enough high for the switching transistors in the mixer to perform complete switching. For $V_{lo,dif}$ higher than 500 mV_p the switching transistors partly operate in the linear region when they conduct. This also causes a gain reduction.

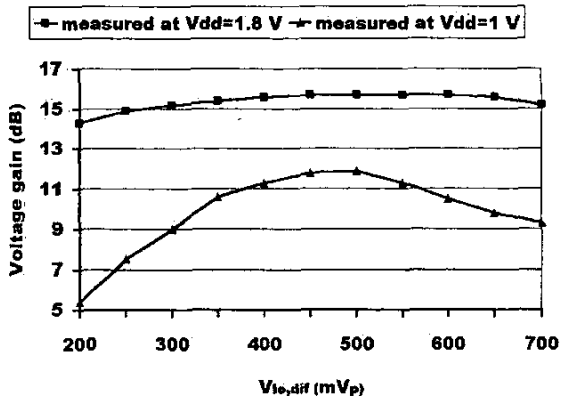

Figure 4. Measured voltage gain versus LO voltage swing

Measured and simulated voltage gain at supply voltages of 1 V and 1.8 V versus frequency are shown in Fig. 5. The difference between the measured and simulated results is mainly due to the parasitic capacitances. Their influence on voltage gain reduction become stronger on the higher frequencies.

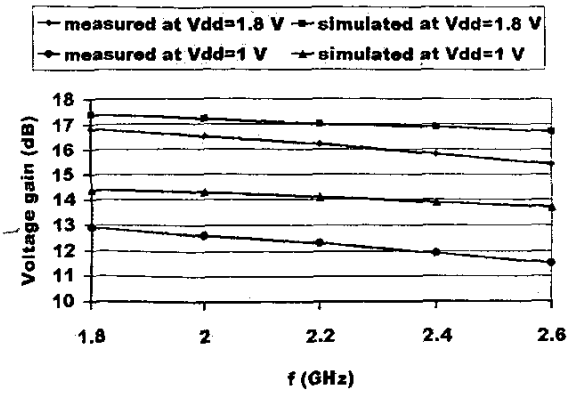

Figure 5. Measured and simulated voltage gain versus frequency

The noise figure (NF) is measured and simulated at IF of 1 MHz, with a 50 Ω source resistance and 1 kΩ load resistance, and with a differential LO voltage swing of 500 mV_p. For LO frequency of 2.4 GHz, a SSB NF of 12.9 dB is measured at a supply voltage of 1.8 V and a SSB NF of 13.9 dB at a supply voltage of 1 V. The measured values for the NF corresponds very well to the simulated results, which are: SSB NF = 12 dB at Vdd = 1.8 V and SSB NF = 13.4 dB at Vdd = 1 V.

Fig. 6 shows a measured $IIP3$ at a supply voltage of 1 V. The simulated $IIP3$ for the same supply voltage is -2.7 dBm. At Vdd = 1.8 V, a measured and simulated $IIP3$ are 1 dBm and 0 dBm, respectively.

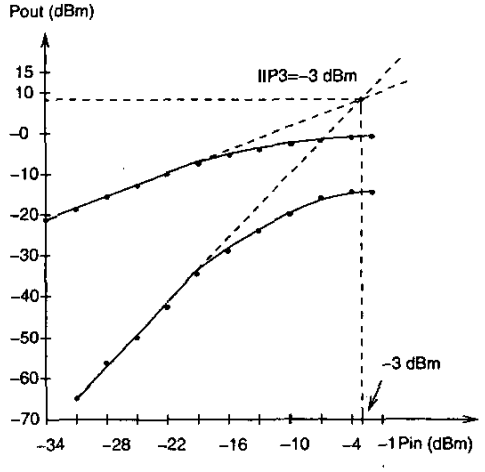

Figure 6. Measured $IIP3$ at a supply voltage of 1 V

In order to evaluate the performance of the folded-switching mixer with current-reuse, the performance of some interesting CMOS mixers are given in Table 1. When comparing the measured performance of the folded-switching mixer with current-reuse with the performance of some CMOS mixers, given in Table 1, the following advantages of the folded-switching mixer with current-reuse can be listed:

Table 1. Performance of some CMOS mixers

Row	Ref.	V_{dd} (V)	I (mA)	NF (dB)	G (dB)	IIP_3 (dBm)
1	[2]	0.9	5.2	13.5	2	3.5
2	[3]	1.8	4.8	10.2	0.5	-6
3	[4]	2	1.5	22	-2.2	6
4	[5]	2	4.1	24	-2.5	21
6	this work	1.8	4.5	12.9	15.7	1
7	this work	1	3.2	13.9	11.9	-3

1. **High voltage gain**

   High mixer voltage gain is important. In a front-end it helps to reduce the noise contribution from building blocks after the mixer. All the mixer implementations presented in Table 1 have significantly lower gain than the folded-switching mixer with current-reuse.

2. **Moderate noise figure**

   Comparing the measured value for the noise figure of the folded-switching mixer with current-reuse with the values for the noise figure of the CMOS mixers given in Table 1, and taking into account power consumption, it is clear that a relatively moderate noise figure is obtained. It is important to take into account for some mixer implementations the fact that they are implemented in older CMOS technologies where the level of thermal and flicker noise was lower. Also some of them use very high intermediate frequency (IF) avoiding the contribution of the flicker noise.

3. **Operation at low supply voltage**

   The presented folded switching mixer with current reuse is performing very well with low supply voltages. Even at the supply voltage of 1 V, a voltage gain of 11.9 dB is measured. Comparing this result with the low voltage mixer presented in [2], it can be seen that the implemented folded-switching mixer with current-reuse has approximately the same noise figure, lower power consumption and much better voltage gain. Only the linearity of the folded-switching mixer with current-reuse is lower compared to the linearity of the mixer presented in [2].

The evaluation of the performance of the folded-switching mixer with current-reuse can be made more clear using a figure of merit for mixers. The figure of merit (Fom) is defined in the following way:

$$Fom = 10\log\left(\frac{10^{G/20}10^{(IIP_3-10)/20}}{10^{NF/10}\cdot P}\right) \qquad (6)$$

Gain (G) and (NF) are expressed in dB and IIP_3 in dBm. The figure of merit is based on the fact that the performance of the mixer is better if NF and power consumption (P) are as low as possible, while gain (G) and IIP_3 are as high as possible. The calculated Fom for the folded-switching mixer with current-reuse and for CMOS mixers from Table 1 is represented in Fig.7. As it can be seen from Fig.7, the folded-switching mixer with current-reuse has the highest Fom, in an absolute sense and outperforms the CMOS mixers represented in Table 1.

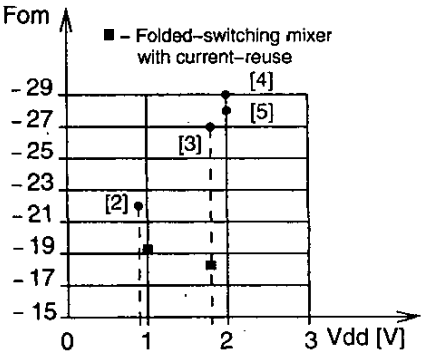

Figure 7. Mixer benchmarking

VI. CONCLUSIONS

A novel, high gain, low voltage, low power folded-switching mixer with current-reuse is designed and implemented. Full insight into the circuit operation is given. This insight is important because it helps a designer to design the folded-switching mixer with current-reuse for different set of specifications. Using the presented measurement results it was shown that the main advantages of the proposed new mixer topology are: high voltage gain, moderate noise figure, operation at low supply voltage and simplicity since the common mode feedback is not necessary. Normalizing mixer performance with a figure of merit shows that the folded-switching mixer with current-reuse has excellent performance in comparison with other CMOS mixers.

ACKNOWLEDGMENT

The authors would like to thank A. Mulders, J. ter Laak, A. Hoogstraate, J. Prummel, J. Otten, F. van Duijvenvoorde from National Semiconductor and Otto Stoelenga from Eindhoven University of Technology for participating in many fruitful discussions, and Technology Foundation STW for the financial support.

REFERENCES

[1] Crols, J., et al., *A 1.5 GHz Highly Linear CMOS Down-conversion Mixer*, IEEE Journal of Solid State Circuits, vol. 30, no. 7, pp. 736–742, 1995.

[2] Debono, C., et al., *A 900 MHz, 0.9 V Low-Power CMOS Downconversion Mixer*, IEEE Custom Integrated Circuit Conference, pp. 527–530, 2001.

[3] Sullivan, P., et al., *Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer*, IEEE Journal of Solid State Circuits, vol. 32, no. 7, pp. 1151–1155, 1997.

[4] Kan, T., et al., *A 2-V 900-MHz CMOS Mixer for GSM receivers*, IEEE International Symposium on Circuits and Systems, vol. I, pp. 327–330, 2000.

[5] Svelto, F., et al.,*A Low-Voltage Topology for CMOS RF Mixers*, IEEE Transactions on Consumer Electronics, vol. 45, no. 2, pp. 299–309, 1999.

[6] Karanicolas, A., et al., *A 2.7-V 900-MHz CMOS LNA and Mixer*, IEEE Journal of Solid State Circuits, vol. 31, no. 12, pp. 1939–1944, 1996.

[7] Vidojkovic, V., et al.,*Mixer Topology Selection for a 1.8-2.5 GHz Multi-Standard Front-End in 0.18 um CMOS*, International Symposium on Circuits and Systems (ISCAS), 2003.