A FREQUENCY OFFSET RECOVERY ALGORITHM FOR CRYSTAL-LESS TRANSMITTERS

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ABSTRACT

In the growing market of low-cost, low data-rate wireless applications there is a significant motivation to implement crystal-less wireless nodes, which will reduce costs and form factor. Several applications benefit from an asymmetric wireless scenario in which the transmitter is required to be cheap, small and ultra-low power, while the receiver will be a residential gateway (RG) or a basestation with a virtually unlimited power budget and relatively higher allowable cost and form factor. In this scenario, while the transmitter will be implemented as a crystal-less node, all the required complexity in the frequency synchronization can be shifted to the RG. Nevertheless the acquisition time should be short compared to the transmission time to save power in the transmitter, and frequency offset in the MHz range should be reduced to few kHz. A new algorithm, which can easily recover frequency offsets larger than the data-rate and which can address the aforementioned issues, is proposed in this paper.

I. INTRODUCTION

The area of low bit-rate communications for applications such as ambient intelligence, sensor networking, and control functions in the consumer home of the future requires wireless solutions with a small size, a lower power consumption and low module costs. Different scenarios can be foreseen regarding the aforementioned applications.

One of these scenarios is constituted by several nodes that are able to transmit data at a low data-rate (few kilobit per second with a duty-cycle lower than 0.1%), and an RG collecting the data for further processing. The RG can communicate with other RGs or a local computer by means of a high data rate wired, as well as a wireless, connection and it is assumed to be mains supplied. Communication between wireless nodes and RGs will be held in the Industrial, Scientific and Medical (ISM) bands to avoid any license costs to the user.

In wireless applications the required accurate frequency synchronization between transmitter and receiver is obtained by using a quartz crystal, which is often used in a crystal oscillator. While in high-end costly application areas, such as cellular telephones and television, the cost of a crystal accounts for no more than 1% of the product cost, in low-end applications the crystal cost can account for as much as 10% of the unit cost. In the recent years solutions other than a crystal based frequency reference have been proposed such as Bulk Acoustic Resonator (BAR) [1] or Micro Electro-Mechanical System (MEMS).

Unfortunately, these solutions present several drawbacks such as high bias voltages and non-standard IC process steps. Therefore, there is a strong economical motivation behind the need to implement a wireless node, which can assure reliable communication without the use of a crystal.

In the aforementioned asymmetric scenario, the TX node will be crystal-less while the frequency synchronization will be achieved at the receiver side by using a dedicated algorithm. The only constraint on the frequency accuracy of the TX node will come from the need to satisfy FCC rules. This means that all the channels should be inside the specified ISM band. This generally translates in a frequency accuracy between 0.1% and 1%, which can be achieved without using a crystal (for example by factory calibration or on-chip calibrated references in commercially available low-power microprocessors)[2].

II. SYSTEM-LEVEL CONSIDERATIONS

ISM bands are generally crowded and present a huge level of interferences. Furthermore multipath fading is pronounced especially in the indoor environment. Therefore, to cope with the non-ideal channel, as well as with multipath fading, and to reduce probability of collision when more wireless nodes transmit at the same time, Spread Spectrum (SS) techniques are commonly employed.

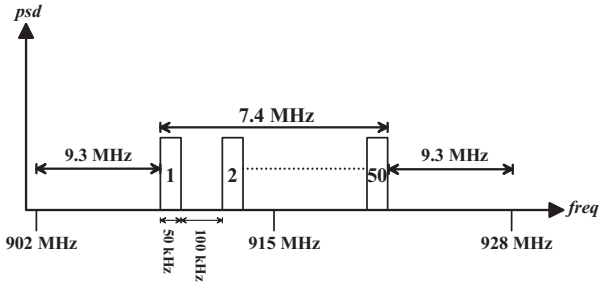

Figure 1: Proposed channel allocation scheme for the 902-928 MHz ISM band

Among different SS techniques, due to shorter acquisition time and the capability to avoid jammed or deep faded portions of the allowed spectrum, an FHSS system is the most suitable SS technique for low data-rate applications in the indoor environment.

Considering for example the 902-928 MHz ISM band, FCC rules set a minimum of 50 hopping channels [3] for any system employing FHSS technique , if intelligent hopping has to be avoided. Indeed, intelligent hopping will translate in a higher transmitter complexity and therefore in a higher over-

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all power consumption. Due to the low data-rate requirement (<10 kbps), considering a BFSK modulation technique with modulation index bigger than 4, a 50 kHz channel bandwidth is a good choice for the intended system. Now, considering 100 kHz frequency distance between adjacent channels to alleviate constraints on the Local Oscillator (LO) phase noise, then the occupied bandwidth is approximately 7.4 MHz. The proposed channel allocation scheme is shown in Fig. 1. As can be seen from Fig. 1, the occupied bandwidth can shift to the left or to the right by more than 9 MHz. This means that the TX and RX local oscillator center frequencies can differ by more than 9 MHz, while FCC rules are still fulfilled.

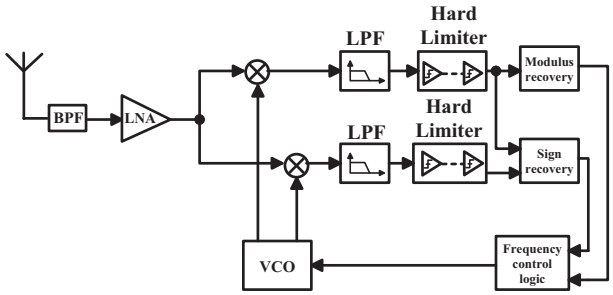


Figure 2: Direct-conversion architecture with frequency offset recovery circuitry

Therefore, the accuracy requirement for the frequency reference at the transmitter side is approximately equal to 1%. Such a requirement for frequency accuracy allows to avoid the use of a crystal. In this way not only costs can be reduced but also the form factor will be greatly improved. Even though the crystal-less transmitter will fulfill the FCC rules, it is important to notice that for a successful recovery of the transmitted data at the receiver side, the offset between the TX and RX local oscillators should be corrected. Several methods exist to recover the frequency offset [4][5], but they make use of the phase information embedded in the transmitted signal and therefore, they can recover frequency offsets smaller than the data-rate. For low data-rate applications a new approach is required, which can recover frequency offsets much larger than the data-rate.
Another possibility is to use a PLL loop and, after the calibration process has been completed, to trap the tuning information on the main capacitor of the loop filter [6]. This approach will anyhow require a PLL, and depending on the size of the packet sent, it is possible that the required storage capacitance can be large. This will increase chip area and therefore device costs.

III. Frequency Offset Acquisition Algorithm

The frequency offset recovery algorithm [7] is used in a direct-conversion receiver architecture and its schematic block diagram is shown in Fig. 2. At the beginning of the transmission, the TX node will send a pilot tone at the carrier frequency. This pilot tone is then mixed down in quadrature with the receiver LO frequency, which is supposed to be at the beginning of the process in the middle of the ISM band. Generally the mixing products contain two components. One component has a frequency equal to the sum of the mixing tones while the second component is equal to the difference between the same tones. While the first component is filtered out by the Low-Pass Filter (LPF), the second one contains the information about the frequency offset between the TX and RX LOs.
The frequency offset acquisition is obtained evaluating the modulus and the sign of the offset. Furthermore, the phase of the incoming signal is also unknown and the recovery algorithm should be able to compensate also for it. The frequency component at the output of the LPF will range within ± 9 MHz. This frequency component can be depicted in the I-Q plane for different initial phase (Φ_1 to Φ_4) as shown in Fig. 3.

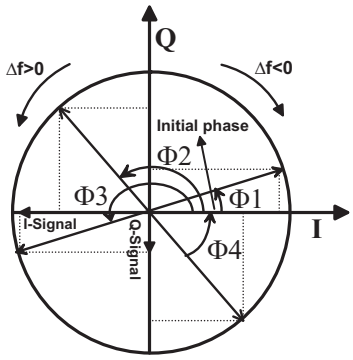
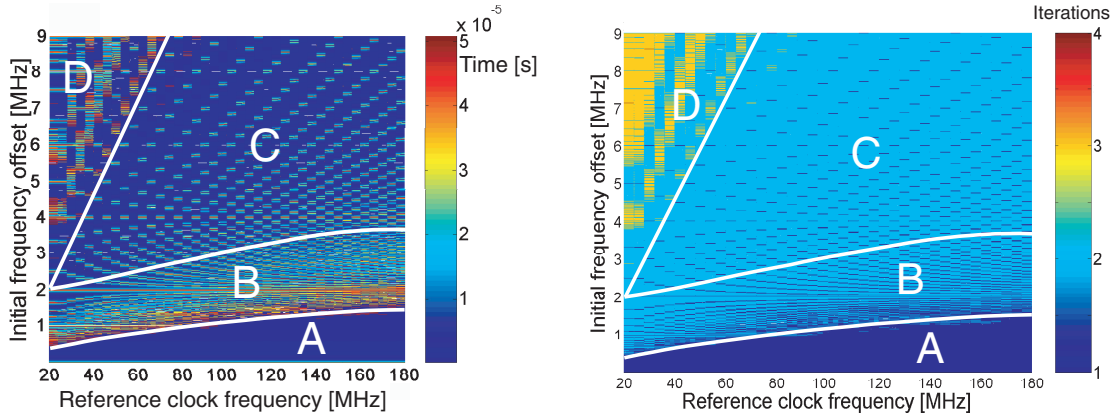


Figure 3: I-Q plane representation of the frequency offset component with different initial phases

The speed at which the phasor rotates is the frequency offset modulus, while the direction of the rotation gives the sign of the frequency offset. The latter information allows the frequency control logic in Fig. 2 to increase or decrease the VCO control voltage by an amount proportional to the frequency offset modulus, increasing or decreasing accordingly the VCO frequency.
If the phasor rotates clockwise, then the difference between the TX carrier frequency and the RX LO frequency is negative, while if the phasor rotates counter-clockwise the same difference is positive and this does not depend on the initial phase of the incoming tone. A flow chart of the implemented algorithm is shown in Fig. 5.
The evaluation of the modulus requires at the receiver side a fast and accurate reference clock. Due to the fact that the RG will be mains supplied and costs can be higher than the TX costs by some order of magnitude, its implementation does not pose any problem. The reference clock at the RG should be fast enough to reduce the error in the evaluation of the frequency offset modulus to a negligible value. Indeed if N is the number of reference clock periods contained in half of the frequency offset signal period, then this value in reality can be N$\pm$1 due to the initial phase difference between the two signals. The error in the estimation of the frequency offset modulus, at each iteration, can be upper bounded the following relation:

$$\Delta \mathrm{f} \simeq \frac{\mathrm{f_{ref}}}{2\mathrm{N}^2} \tag{1}$$



(a) Acquisition time (b) Number of iterations

Figure 4: Iteration number and acquisition time vs. reference clock frequency (initial offset ∈ [10 kHz, 9 MHz])

while the estimated frequency offset modulus is:

$$| \, f_{off} \, | = \frac{f_{ref}}{2N} \tag{2}$$

where f_{ref} is the frequency of the reference clock.

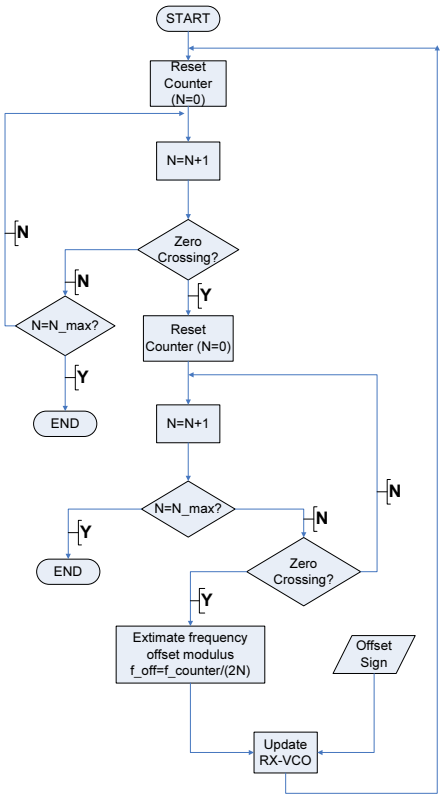


Figure 5: Frequency offset recovery method flowchart

The choice of the optimal reference clock frequency is not trivial. It is necessary to minimize the acquisition time to minimize the transmitter power consumption. In Fig. 4(a) the acquisition time versus the initial frequency offset and the reference clock frequency is plotted. Four different regions are visible. In the region A, the required time is roughly constant and independent from the frequency of the reference clock. Indeed, for small initial frequency offsets, the acquisition time depends from the offset value itself and the algorithm is repeated only one time to reach the required accuracy in the frequency acquisition. This is visible in Fig. 4(b). Of course, the higher the reference clock frequency, the wider the initial frequency offset range that requires a single iteration to achieve the required accuracy.

In the region B, the initial frequency offset requires more iterations, generally two, sometimes one. Increasing the reference clock frequency leads to a more accurate estimation at the first iteration but never accurately enough. Therefore, a second iteration is needed, but due to the more accurate first acquisition, the second iteration will require more time. Therefore, this area tends to enlarge increasing the reference clock frequency.

The area C requires between one and two iterations (mainly two). This is the area which requires the smallest acquisition time (excluding the A area) and it tends to enlarge increasing the reference clock frequency. Obviously, the initial frequency offset is so large that the first acquisition is almost never sufficient. On the other hand, when a second iteration is required, it does not take large time. Indeed, in the first acquisition the residual offset is still large enough requiring less time to reach the wanted accuracy.

Finally, the region D is dominated by the large number of iterations required (mainly three iterations). In this case the reference clock frequency is too small. Therefore, the first iterations are very inaccurate requiring the algorithm to be repeated more than two times.

The criteria in the choice of the optimal reference clock frequency is based on the minimization of the average acquisition time for several transmitters. Considering the initial frequency offset uniformly distributed, and the whole frequency offset range subdivided in "k" slots, then the average acquisition time is

$$\mathrm{Time}_{avg} = \frac{1}{\Delta f_{off}} \sum_{i=1}^{k} T_{acq,k} \Delta f_k \tag{3}$$

where Δf_{off} is the initial frequency offset range, $T_{acq,k}$ is the acquisition time in the k^{th} frequency slot and Δf_k the

Table 1: I and Q-signal transitions for initial phase difference between TX and RX oscillators $\in [0,\pi]$

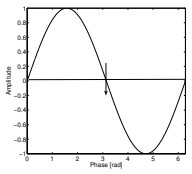
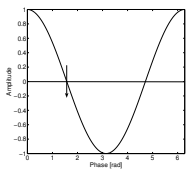
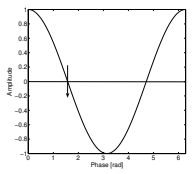
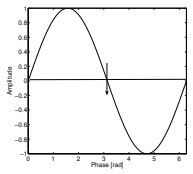
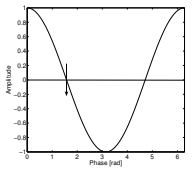
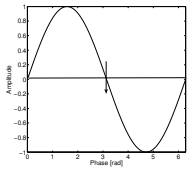
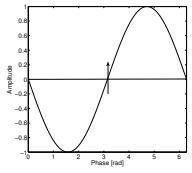
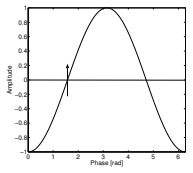
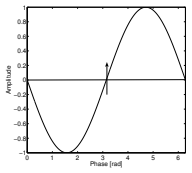
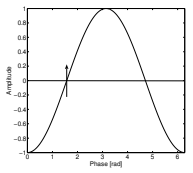
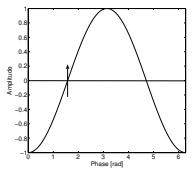
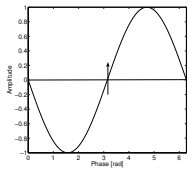
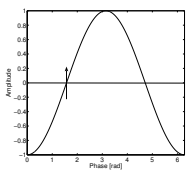
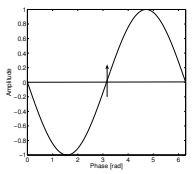
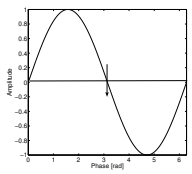
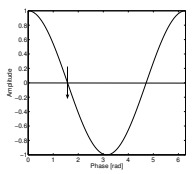
Signal	***[0,*** $\frac{\pi}{2}$***],*** $\Delta f > 0$	***[0,*** $\frac{\pi}{2}$***],*** $\Delta f < 0$	***[*** $\frac{\pi}{2}$***,*** π***],*** $\Delta f > 0$	***[*** $\frac{\pi}{2}$***,*** π***],*** $\Delta f < 0$
$Q - Signal$				
$I - Signal$				

Table 2: I and Q-signal transitions for initial phase difference between TX and RX oscillators $\in [\pi,2\pi]$

Signal	***[*** π***,*** $\frac{3\pi}{2}$***],*** $\Delta f > 0$	***[*** π***,*** $\frac{3\pi}{2}$***],*** $\Delta f < 0$	***[*** $\frac{3\pi}{2}$***,*** 2π***],*** $\Delta f > 0$	***[*** $\frac{3\pi}{2}$***,*** 2π***],*** $\Delta f < 0$
$Q - Signal$				
$I - Signal$				

frequency width of the k slots. A picture of the average acquisition time versus the reference clock frequency is shown in Fig. 6.

The minimum average acquisition time is obtained for a reference clock frequency of around 70 MHz. The time required to reduced the initial frequency offset below the wanted maximum value is in any case less than 50 μs (see Fig. 4(a)). Then, to complete the acquisition process, it is necessary to wait one more iteration as can be seen looking at Fig. 5. The last iteration will produce an overflow on the counter (the counter reaches $\mathrm{N_{max}}$), which will end the acquisition process. Considering a 70 MHz reference clock frequency and a 5 kHz maximum residual frequency error, then a 14-bit counter is required. This will require around 230 μs to produce an overflow. Therefore, the complete acquisition process requires less than 300 μs to be accomplished. At 10 kbps this is equivalent to 3 bits data overhead, which is a reasonable value in terms of energy consumption.

The next step in the proposed algorithm deals with the recovery of the frequency offset sign. For this, quadrature down-conversion is needed. To understand the basic principle behind the algorithm it is useful to look at Table 1 and Table 2. Supposing to look only at the transition type (which means in Fig. 3 when a phasor crosses the I or the Q axis), it is possible to have two situations, which leads to the same output even when the sign of the frequency offset is opposite. Indeed, looking at Table 1 and Table 2, independently from the initial phase difference between the incoming signal and the LO synthesized frequency, the frequency offset component experiences the same type of transitions either when the frequency offset is positive or it is negative. Therefore, to correctly evaluate the frequency offset sign independently of the initial phase difference between the incoming pilot tone and the RX LO synthesized frequency, additional information is needed.

Looking at Table 1 or Table 2, the required information can be found in the time. Indeed when, for example, Δf>0 and the initial phase is between 0 and $\frac{\pi}{2}$ (Table 1, 1$^{\mathrm{st}}$ column), the Q signal crosses the zero (I axis in the I-Q plane) always after the I signal. In the first column of Table 1 an initial phase difference of zero radians has been supposed. When Δf<0, the Q signal crosses the I axis always before the I signal. Therefore, when Δf>0 and the initial phase difference is between 0 and $\frac{\pi}{2}$ the Q-signal lags and the I-signal leads, while when Δf<0, even though the transition of the I and Q signal are still both negative, the I signal lags and the Q signal

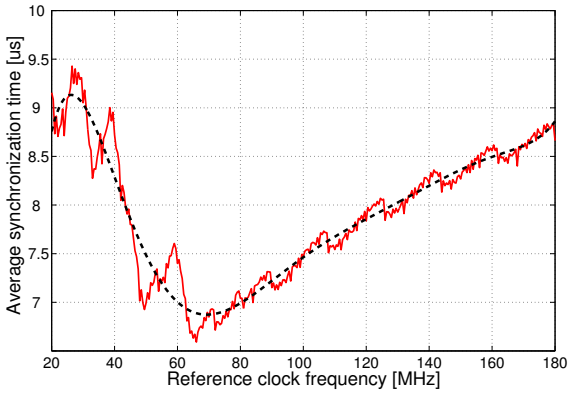


Figure 6: Average acquisition time vs. reference clock frequency

leads (the initial phase difference in Table 1, 2nd column is $\frac{\pi}{2}$). The same considerations can be applied for the other possible phase relation ranges shown in Table 1 and Table 2, in which initial phase difference has been chosen to highlight the leading and the lagging signal components. The evaluation process is summarized by the flowchart in Fig. 7.

IV. Implementation and Simulation Results

To test the proposed algorithm, a full wireless link has been implemented using Simulink^{TM}. The modulus recovery circuitry has been implemented using a 14-bit counter and two D-Flip-Flops (D-FF) and a few logic ports. The sign recovery circuitry requires only 16 D-FFs and a few logic ports. Simulations show that starting from 9 MHz frequency error between TX and RX LOs, which corresponds to approximately 1% frequency accuracy, the frequency offset can be lowered in two steps to less than 6 kHz (6.5 ppm) in less than 300 μs.

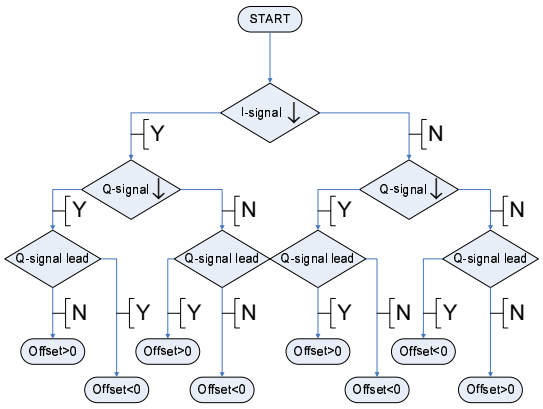


Figure 7: Frequency offset sign recovery method flowchart

In Fig. 8 the frequency offset signal is plotted versus the recovery time. At the beginning of the acquisition process, the frequency offset is in the order of MHz (1.58 MHz). After the first correction the frequency is 916.556 MHz. The frequency difference is still too large and therefore a second iteration is needed. At the end of the calibration process the synthesized frequency at the receiver side is 916.5804 MHz, which is only 400 Hz far from the TX carrier frequency (916.58 MHz). The inset of Fig. 8 shows the downconverted residual frequency error during the calibration process (at the output of the receiver mixers). The required acquisition time is approximately 42 μs (Fig. 8) excluding the last iteration (around 230 μs).

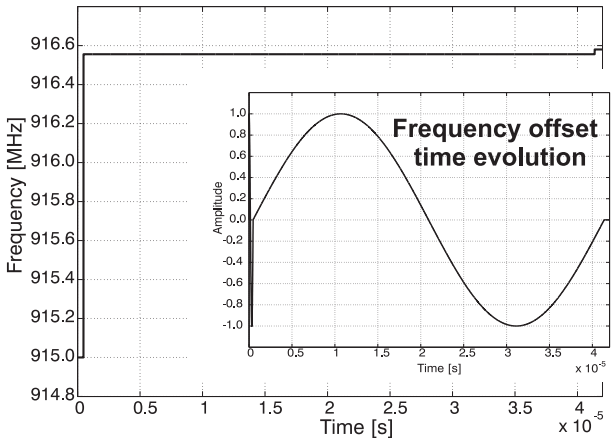


Figure 8: Receiver synthesized frequency vs time

V. Conclusions

An approach to implement a crystal-less transmitter in an asymmetric scenario (many TX sending to a mains supplied RG) has been described. Getting advantage from the low data-rate requirements it has been proven that frequency accuracy at the transmitter side can be relaxed to a point at which no crystal is needed. At the same time the RG will align its center frequency to the transmitter center frequency by using a dedicated algorithm.

This algorithm can be implemented mainly in the digital domain and requires the transmitter to send a pilot tone for no more than 300 μs. This will negligibly affect the power consumption at the transmitter side given a data-rate lower than 10 kbps. Simulations have proven that frequency offsets up to $\pm$9 MHz can be reduced to less than 6 kHz, which corresponds to a frequency accuracy better than 6.5 ppm.

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