A 60µW/180µW Digitally Controlled Switched-Cap LC Oscillator for 900MHz/2.4GHz operation

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***Abstract*— An LC-tank oscillator for ultra-low-power narrow-band applications is designed using a switched capacitors tuning implementation in a 9-layer-metal 90nm RF CMOS technology. The oscillator is targeted for 900MHz and 2.4GHz ISM bands operation with external inductors. The design resulted in a flexible and digitally controllable oscillator core that can be used with both external and planar integrated inductors. The presented VCO consumes 60µW in the 900MHz band and 180µW in the 2.4GHz band from a 1.2-V power supply. The best simulated phase noise at 1.5MHz is -121dBc/Hz and -131.8dBc/Hz in the 2.4GHz band and in the 900MHz band, respectively. A highlight of this design is the fact that an excellent Figure-of-Merit (ranging from -193dB to -199dB) is combined with a very large tuning range (>16% in both operational bands).**

I. INTRODUCTION

The most important and demanding parameters of an efficient oscillator are power consumption, frequency tuning range and phase noise. In LC-tank oscillators phase noise and power consumption depend primarily on the quality factor of the tank and on the nonlinearities of the varactors. Moreover, the frequency tuning range is determined by the tuning range of the varactors. In order to improve the oscillator performances and to meet tuning range requirements that integrated varactors may not provide, a band-switching implementation is considered for this design. Different from circuits presented in literature [1]-[3], where band-switching is used together with integrated varactors, the presented LC-tank oscillator is designed considering only digitally controlled switched capacitor banks, used to obtain a discrete passive capacitive tuning, and offering wide tuning ranges and high tank quality factors.

Section II and Section III describe in detail the design issues and, in particular, the design of switched capacitor bank. Simulation results are then discussed and compared to the state of the art in Section IV.

II. DESIGN ISSUES

Accurate specifications are always dependent on application and system constraints. In particular, the presented VCO shows suitable performance to be employed in low-bit rate narrowband FSK modulated systems [4].

The dual band operation (2.4GHz and 900MHz) is accomplished by using the same oscillator core, composed by a current source, an active part and a switched capacitor bank, but a different inductor value for each band. For the 2.4GHz band, the inductance of bonding wires is used to obtain a total value $L_{2.4GHz}$=3nH (assumed Q_L=50). For the 900MHz band, external coils (PCB tracks) are used with a total value L_{900MHz}=20nH (assumed Q_L=50).

The schematic diagram of the current source and the active part of the designed oscillator is shown in Fig.1. The voltage supply is fixed at 1.2-V. A complementary MOS cross-coupled pair topology provides a negative modelled resistance $-1/g_m$ in order to compensate for the losses in the tank circuit. As such, the Barkhausen conditions for start-up and steady-state oscillation are met. The use of a complementary cross-coupled pair doubles the total differential transconductance $0.5*(g_{m\_n}+g_{m\_p})$ compared to a single cross-coupled pair implementation. Moreover, due to the fully symmetrical topology, it results in a low $f_{1/f}$ corner of the phase-noise [5].

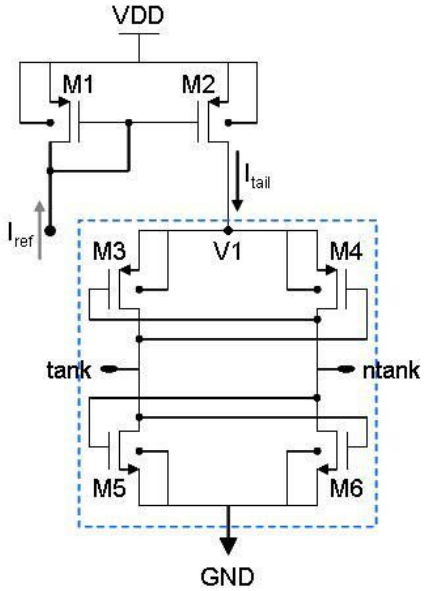

Fig. 1 Schematic view of the current source and of the complementary MOS cross-coupled pairs used as active part.

A disadvantage of the complementary implementation is the higher level of parasitics from the active part. This reduces the frequency tuning range. On the other hand, the

complementary topology represents a trade-off between all n-MOS and all p-MOS cross-coupled implementation in order to achieve a good phase noise combined with ultra-low-power consumption [3].

In order to start the oscillation, a minimum negative transconductance is required in each band: it has been calculated as $1/R_{PAR}$, where:

$$R_{PAR} = \frac{R_C * (1+Q_C^{\,2}) * R_L * (1+Q_L^{\,2})}{R_C * (1+Q_C^{\,2}) + R_L * (1+Q_L^{\,2})} \qquad (1)$$

being Q_C and R_C the capacitive bank quality factor and the corresponding parasitic series resistance, and Q_L and R_L the inductor quality factor and the corresponding parasitic series resistance, respectively [5]. Based on (1) and in order to get the best trade-off between an ultra-low power consumption requirements and good phase-noise performances, I_{ref} is fixed to 10µA and 30µA, for the 900MHz and the 2.4GHz band, respectively.

III. SWITCHED CAPACITOR BANK

In the presented LC oscillator switched capacitor banks are controlled by 7bits of digital tuning voltage such that the minimum frequency step equals 32 kHz, in the 900MHz band, and 78 kHz, in the 2.4GHz band. Moreover, the high Q of the capacitor bank results in a very good phase-noise performance. On the other hand, the use of a switched capacitor bank does result in a larger chip area and extra parasitics due to the size and the complexity of the bank. This reduces the frequency tuning range. In addition, we need to provide for some overlap between discrete frequency bands in order to avoid frequency gaps.

The differential implementation of the switched capacitor is shown in Fig. 2, together with the simplified on-state and off-state models. It represents the unit cell of the capacitor bank.

In the on-state, resistance R_{sw_ON} needs to be minimized in order to maintain a high Q:

$$Q = \frac{1}{\omega C_{sw} R_{sw\_ON}} \qquad (2)$$

where C_{sw} is the series connection of C1 and C2. In the off-state, the parasitic capacitance of the switch C_{sw_OFF} is dominant in the series connection with C_{sw}. Therefore it should be minimized in order not to reduce the effective tuning range of the bank.

Metal-Oxide-Metal (MOM) caps with three metal layers (ME4-ME6) are used, in the present design. The lower resistivity of the higher metal layers limits reducing both parasitic capacitances and parasitic resistances. In general, a careful layout of the capacitor bank is mandatory in order to prevent parasitics from degrading the oscillator performance.

The approach used to build the 7bits switched capacitor bank is to multiply the unit cell, that constitutes the LSB, by 2, 4, 8, 16, 32, and 64 in order to obtain seven blocks connected in parallel. Each of them is controlled by 1bit of the digital tuning. The multiplication of the unit cell is expected to provide good results for matching, but it is costing in terms of area.

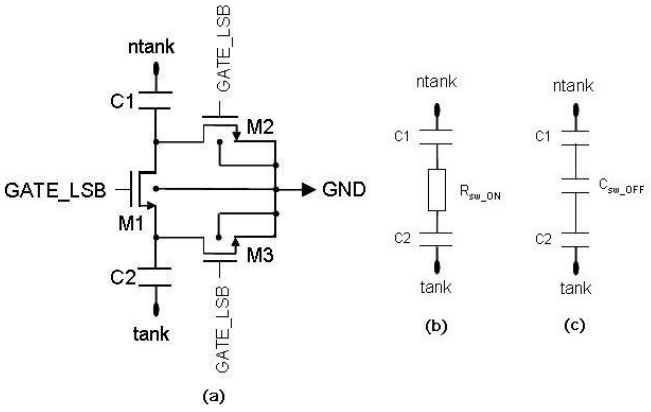

Fig. 2 Schematic diagram and on/off model of the differential switched capacitor.

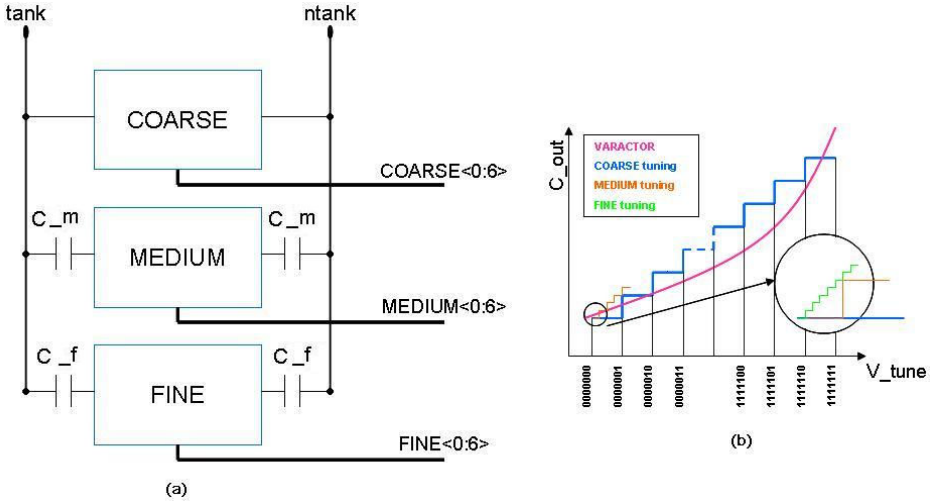

Fig. 3 Block diagram of the total capacitor bank (a) composed by the coarse, the medium, and the fine tuning banks. Discrete tuning obtained by mean coarse, medium and fine tuning is illustrated in (b).

The basic idea of using a switched capacitor bank is to replace the continuous capacitance variation of a tuned varactor, by the discrete tuning of a switching capacitors bank. The main challenges of this approach are the minimum frequency step achievable and the band overlapping. In order to reduce the minimum step, the same capacitor bank is connected in series with two small capacitances (to keep the symmetry of the system). The series connection lowers the capacitive contribution of the bank at each tuning step. For this design both a medium tuning bank and a fine tuning bank have been connected in parallel to the coarse one.

The block diagram of the resulting total capacitor bank is shown in Fig.3 together with a simplified plot describing the discrete tuning mechanism. Each bank is controlled by an independent 7 bits and MIM caps are used for the series output capacitances. The band overlapping requires that the ΔC due to a full sweep of the fine tuning bank (from 0000000 to 1111111) must be higher than the ΔC due to a single step of the medium tuning bank (from 0000000 to 0000001). At the same time, the ΔC due to a full sweep of the medium tuning bank (from 0000000 to 1111111) must be higher than the ΔC due to a single step of the coarse tuning bank (from 0000000 to 0000001).

The simulated capacitance overlapping results are summarized in Table 1; minimum frequency steps of 32KHz and 78KHz are obtained in the 900MHz and in the 2.4GHz bands, respectively.

TABLE I
SIMULATED CAPACITANCE OVERLAPPING RESULTS

$\Delta C_{FINE\_fullswep}$	27.1e-17
$\Delta C_{MEDIUM\_onestep}$	5.1e-17
$\Delta C_{MEDIUM\_fullsweep}$	6.53e-15
$\Delta C_{COARSE\_onestep}$	3.84e-15

IV. SIMULATION RESULTS

In the following, the OFFstate and the ONstate nomenclature is used to describe two opposite conditions for the switched-cap bank. In particular:

- OFFstate: all control bits (coarse, medium and fine tuning) are set to 0 (zero) causing the cap bank to be in the switched OFF state. In this state the cap bank provides the minimum capacitive load and, as a consequence, the maximum frequency of the tuning range is achieved in each band;
- ONstate: all control bits (coarse, medium and fine tuning) are set to 1 causing the cap bank to be in the switched ON state. In this state the cap bank provides the maximum capacitive load and, as a consequence, the minimum frequency of the tuning range is achieved in each band.

A transient simulation in the 2.4GHz band is shown in Fig.4. The start-up time of the system is 150ns. The VCO is tuneable from 2.2GHz to 2.63GHz corresponding to a tuning range of 17.9%. Power consumption is 180µW from a 1.2-V power supply. The best simulated phase noise is -121dBc/Hz at 1.5MHz offset.

A transient simulation in the 900Mz band is shown in Fig.5: the VCO is tuneable from 861MHz to 1.01GHz corresponding to a tuning range of 16.5%.

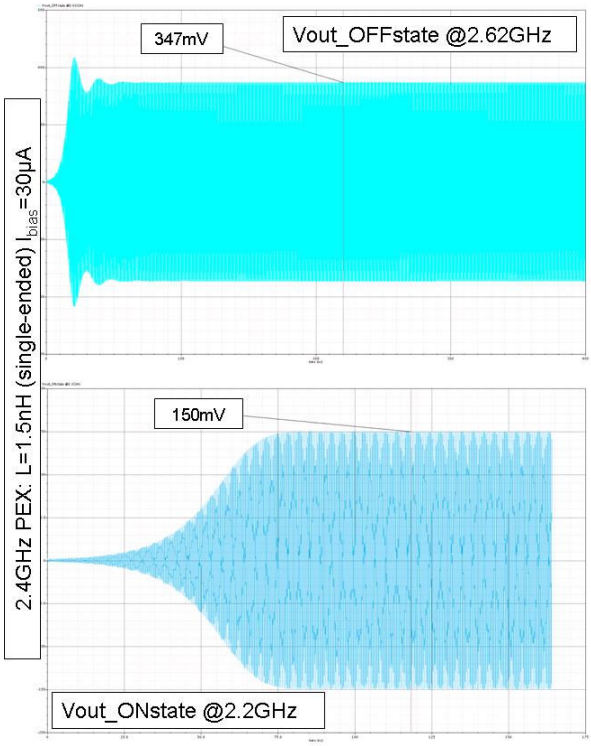

Fig.4 Transient response for the minimum and maximum frequency in the 2.4GHz band when a bias current I_{bias}=30µA is used.

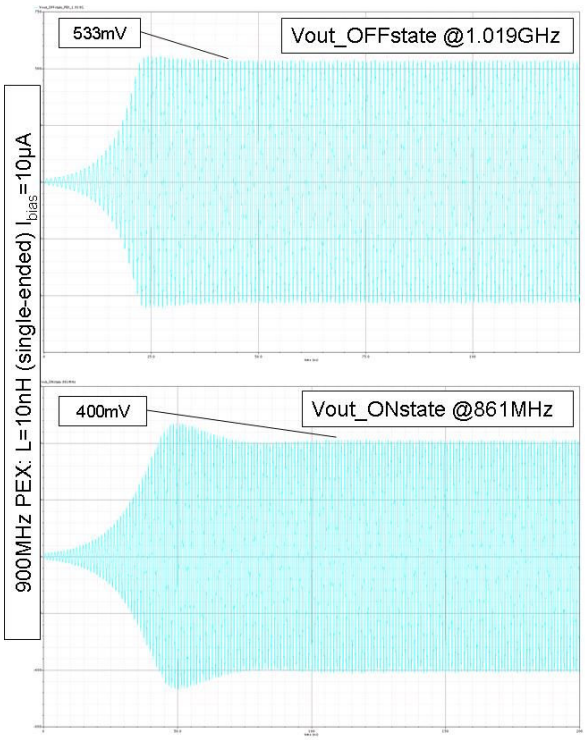

Fig. 5 Transient response for the minimum and maximum frequency in the 900MHz band when a bias current I_{bias}=10µA is used.

TABLE II
VCO PERFORMANCE SUMMAY AND COMPARISON WITH PUBLISHED WORKS

Reference	Technology	Oscillating Frequency (GHz)	Phase Noise (dBc/Hz)	Power P_{DC}	FOM (dB)
This work 2.4GHz band	RF CMOS 90nm bond-wires	2.2-2.63 (17.9%)	@1.5MHz -117 -121	180 µW	-187.7 -193.4
This work 900MHz band	RF CMOS 90nm external coils	0.861-1.01 (16.5%)	@1.5MHz -131.8 -125	60 µW	-199.2 -193.8
[3]	CMOS 0.18µm on-chip	2.4-2.44 (1.66%)	@1MHz -134	4.6 mW	-195
[6]	CMOS 0.18 µm on-chip	0.825-0.975 (16.6%)	@3MHz -136	2.4 mW QVCO	-180
[7]	CMOS 0.18 µm bond-wires	1.87 (8.3%)	@1MHz -114	100 µW	-190
[8]	CMOS 0.13µm on-chip	2.2 (13.6%)	@1MHz -110.7	600 µW QVCO	-179.7

In this case, the power consumption is 60µW from a 1.2-V power supply. The best simulated phase noise is -131.8dBc/Hz at 1.5MHz offset. The start-up time of the oscillator is 100ns.

In order to compare the presented VCO performance to other published work, it is useful to employ a figure-of-merit (FOM) that captures two important performance parameters for oscillators: phase noise and power consumption. The following formula is used here to calculate FOM:

$$FOM = L\{f_{offset}\} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (3)$$

where $L\{f_{offset}\}$ is the simulated phase noise at 1.5MHz offset from the carrier frequency f_0 and P_{DC} is the oscillator power consumption in mW. Nevertheless, the tuning range of the VCO is not taken into account in (3). The combination of an excellent FOM with a large tuning range (>16% in both operational bands) represents a highlight of the presented VCO.

The oscillator performance is summarized and compared with other published low power VCOs in Table 2.

V. EXPERIMENTAL RESULTS

The described digitally controlled switched-cap LC oscillator has been developed in 9-layer-metal 90nm RF CMOS technology. At the moment of writing, measurements of the VCO performance are still ongoing.

VI. CONCLUSIONS

This paper presents a dual band (2.4GHz and 900MHz) ultra low power, completely digitally tuned with a frequency-resolution below 100KHz, switched-cap oscillator designed in 90nm RF CMOS. Bond-wires inductors and PCB traces are employed for high Q and they are used for the 2.4GHz band and for the 900MHz band, respectively. A large tuning range is achieved in both operational bands, thanks to the switched-cap bank topology. Moreover, this results in a flexible design that can be used with both external and planar inductors. The calculated power consumption is lower or comparable to other state-of-the-art designs. The same is true for the FOM, even while the excellent FOM is combined with a large tuning range.

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